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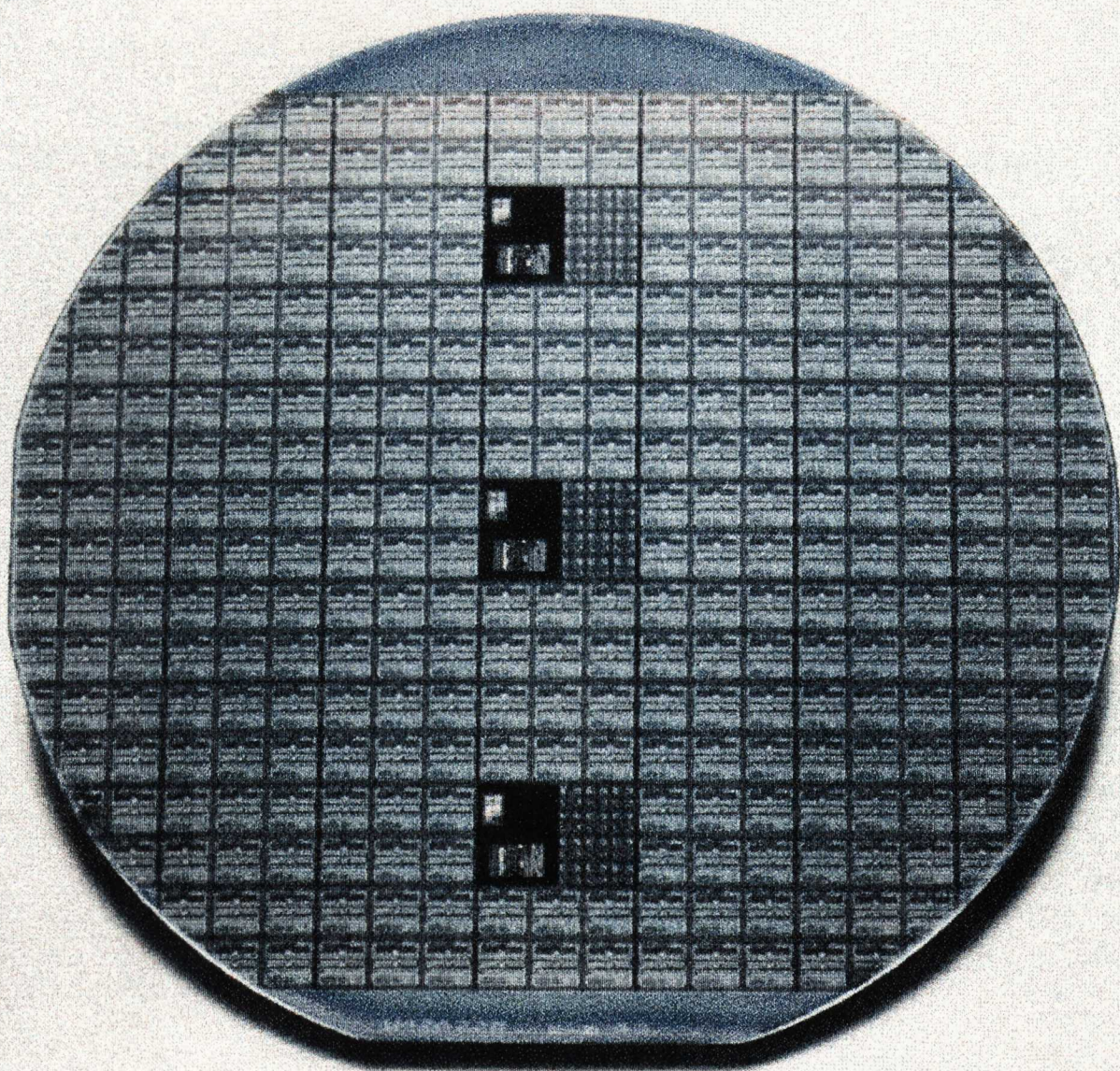
The adoption of Application Specific Integrated Circuit (ASIC) technology by the UK manufacturing base.

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**Submitted for the degree of Doctor of Philosophy
Faculty of Technology
The Open University**

September 1997

APPENDICES
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A six-inch wafer containing mixed-signal ASICs

This work is dedicated to my wife Ann without whose constant support and encouragement it would not have been possible.

'Everything has been thought of before, but the problem is to think of it again'

J.W von Goethe. 1779

*'There is one thing stronger than all the armies in the world: and that is an
idea whose time has come'*

Victor Hugo. 1875

Acknowledgments.

I would like to thank a number of people who have been of great help and assistance in producing this study. The list is long and I apologise for omissions:

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- My colleagues at Plextek Ltd. for acting as a useful sounding board for ideas, and our clients who have provided much of the inspiration and example of the successful adoption of microelectronic technology

Abstract.

Since the late 1970s, families of microelectronic technologies that could bring the advantages of high levels of electronic integration have been available at reasonable prices and manageable risk to all sectors of UK industry. However, the uptake of these technologies has been painfully slow, particularly by the small and medium enterprises (SMEs) that make up most of the companies currently operating in the UK. It is the aim of the research described here to assess how slow the uptake has been, the reasons for it, and possible solutions to the problem. The problem is investigated with reference to SMEs.

In order to reach conclusions it has been necessary to :-

- Define Application Specific Integrated Circuit (ASIC) technology and review its history
- Review that nature of the UK SME base and identify why they should use ASICs
- Review the UK, European and World ASIC markets
- Analyse the nature of the UK ASIC design and supply industry
- Ascertain the reasons for non-adoption and assess their validity
- Relate the findings of this research to appropriate business, organisational and system models
- Review past and existing technology-transfer programmes operating in the area of ASIC adoption at a UK, European and world level
- Compare the adoption of ASIC technology with the adoption of similar, wide-ranging, new technologies

The study concludes that the technology is unique in the wide range of industries to which it can be applied, and that although some advances in adoption have been made, there remains a significant number of hurdles to adoption which can best be addressed by government intervention and supporting activity from supply-companies, trade-associations, user-groups and professional and educational institutions. Only once adoption has reached a 'critical mass' can it be assumed that a self-sustaining market will result.

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Glossary.

Antifuse	A structure which programs to a low resistance when a high programming current is passed through it. Used in some forms of FPGA.
ALU	Arithmetic & Logic Unit: The combinatorial processing core of a digital processor (microprocessor, microcontroller etc.).
ASIC	Application-Specific Integrated Circuit.
ASSP	Application Specific Standard Part: Commodity semiconductor chips used in general applications.
CAE	Computer-Aided Engineering: A generic term for the hardware and software tools used in the simulation and layout of ASIC devices, and in other engineering disciplines.
CASE tools	Computer Aided Software Engineering: High-level software tools used in software system design.
CBIC	Cell-Based Integrated Circuit: A type of masked ASIC.
Chip	An integrated circuit

CMOS	Complementary Metal Oxide Semiconductor: The most common fabrication technology for ASICs.
CNC	Computer Numerically Controlled: A term used to describe the electronic control of machine tools.
CPLD	Complex Programmable Logic Device: A generic term used to describe user-programmable logic devices that are slightly lower than FPGAs in complexity.
DNA	Deoxyribonucleic Acid: The molecule of heredity. The purine and pyrimidine bases of DNA carry genetic information.
DRAM	Dynamic Random Access Memory: A semiconductor memory construct based on capacitance which must be continually re-written to maintain its data.
DTI	Department of Trade and Industry: A UK government department.
EMC	Electromagnetic Compatibility: The behaviour of a device in respect of its emissions of and susceptibility to radio frequency interference.

EPROM	Erasable Programmable Read Only Memory: A type of ROM which can have its data erased and re-written using a programming device.
EU	The European Union.
Eurochip	An EU funded programme to develop and supply prototype ASICs for academic and industrial users.
FEI	Federation of Electronic Industries: A trade association
Foundry	A factory that produces integrated circuits, often on a sub-contract basis.
FPGA	Field Programmable Gate Array: A generic term covering a range of programmable logic devices with higher complexity than CPLDs and PLDs.
Gate	The basic building block of digital circuits. A device capable of performing a simple Boolean function (e.g. AND, OR).

Gate Array	An semi-custom digital integrated circuit where customisation is achieved by connecting an array of uncommitted gates using etched metal tracks on the chip.
GSM	A standard for digital mobile telecommunications named after the ‘Groupe Special Mobile’ within ETSI that wrote the standard.
HDL	Hardware Description Language: Text languages used to describe hardware functions (e.g. VHDL, Verilog).
HEI	Higher Education Institutions: Universities and former polytechnics and colleges involved in tertiary education.
IEE	Institution of Electrical Engineers: The UK institution regulating and representing electrical engineers.
IEEE	Institution of Electrical and Electronic Engineers: The USA equivalent of the IEE.
JEDEC	Joint Electronic Device Engineering Council: An international standards body operating within the semiconductor industry.

MAb	Monoclonal Antibody: An antibody that can be produced in large amounts by fusing an antibody producing cell with a myeloma (cancerous) cell.
MiB	Microelectronic in Business: A DTI initiative to increase the adoption of microelectronics in the UK.
Microcontroller	A single chip containing a microprocessor core along with peripheral devices such as program memory (PROM) and random access memory (RAM).
MPW	Multi Project Wafer: A method of lowering NRE charges by sharing space on a wafer between several devices.
Netlist	A text file containing information relating to the connectivity of elements in an electronic circuit
NRE charge	Non-Recurring Engineering charge: A tooling charge made by a semiconductor company for masked ASICs.
OTP ROM	One Time Programmable Read Only Memory: A type of ROM that may be programmed once using a programming device, but cannot be re-written.

PAL	Programmable Array Logic: A simple form of programmable logic device.
PALASM	PAL Assembler: A low-level language for describing the function of PAL devices.
PCB	Printed Circuit Board: A laminated board of copper and insulator which forms electrical connections between components attached to it.
PLD	Programmable Logic Device: A generic term for logic devices which can be programmed by the user (e.g. FPGA, PAL).
PTH	Plated Through Hole: A printed circuit board assembly technique where component leads penetrate the board.
RAM	Random Access Memory: A generic term for semiconductor memory that can be accessed (written to and read from) non-sequentially.
ROM	Read Only Memory: Non-volatile semiconductor memory which cannot be written to when in-circuit.

SBA	Semiconductor Businesses Association: A UK trade-association.
Scan Path	A production test methodology used in many ICs in which test patterns and their results are passed through the device via shift registers.
Slice	See wafer
SME	Small or Medium Enterprise: A company employing fewer than 500 people (250 in the UK by DTI definition).
SMT	Surface Mount Technology: A printed circuit board population technique where components do not penetrate the board.
SPICE	An analogue simulation software-tool used mainly at component level (e.g. transistors, resistors, capacitors)
SRAM	Static Random Access Memory: A semiconductor memory which does not need to be refreshed to retain its data
Turn-key design	A design performed entirely by a third-party.

UART	Universal Asynchronous Receiver/Transmitter: A function, often incorporated in a microcontroller, to interface to an asynchronous communications line (e.g. RS232).
ULA	Uncommitted Logic Array: An early form of bipolar gate array.
Verilog	A hardware description language.
VHDL	The HDL (hardware description language) developed by the US DoD (department of defence) for the VHSIC (very high speed integrated circuit) programme.
Wafer	Also referred to as a slice. A disk of silicon containing a number of chips which is cut into individual die and packaged.
Yield	The percentage of circuits initially fabricated on a slice that pass post-manufacturing tests.
Yourdon	A structured design methodology used in software engineering.

1. Introduction.

1.1 Summary of Study

Since the late 1970s, families of microelectronic technologies that could bring the advantages of high levels of electronic integration have been available at reasonable prices and manageable risk to all sectors of UK industry. However, the uptake of these technologies has been painfully slow, particularly by the small and medium enterprises (SMEs) that make up most of the companies currently operating in the UK. It is the aim of the research described here to assess how slow the uptake has been, the reasons for it, and possible solutions to the problem. The problem is investigated with particular reference to SMEs.

In order to achieve this result it has been necessary to perform a structured research programme which went through the stages outlined below.

1.1.1 Stage 1. Definition of ASIC technology.

The term 'Application Specific Integrated Circuit' (ASIC) is used very loosely in the electronics industry, so before any meaningful research could be undertaken, it was necessary to define the scope of the technology and produce a tighter definition of the sub-categories of ASIC. At this stage it was also useful to review the history of the technology and to review the influence that the history of the technology might have on its adoption by SMEs in the 1990s.

1.1.2 Stage 2. Review of the UK SME base.

‘Small and medium enterprise’ is a popularly used phrase, but its definition varies. Stage two defines the SME in relation to this study, estimates the size of the UK SME base and identifies why SMEs should consider using ASIC technology by reference to marketing models, industry structure and specific case-histories.

1.1.3 Stage 3. Market analysis.

The work of this study rests on the hypothesis that SMEs do not use ASIC to the extent that they might profitably do, or to the extent that their overseas competitors do. So as to prove this hypothesis it was necessary to investigate the size and nature of the UK, European and World ASIC markets, particularly with respect to SMEs. A survey of ASIC design and supply companies was undertaken to support both this stage, and stage 4.

1.1.4 Stage 4. Supply-side analysis.

In order to understand the nature of the market, it was also necessary to analyse the ASIC supply industry. The UK is unusual in the number of small design-companies operating in ASIC technology, so it was necessary to investigate further the nature of the supply industry, again with particular reference to SME users.

1.1.5 Stage 5. Reasons for non-adoption.

Having established that the level of adoption was low, the next stage was to establish the reasons for non-adoption. This was mainly performed by surveys. Having established perceived reasons, each of the major reasons perceived by non-users was analysed so as to identify whether it was based in fact or whether it was a misconception. A survey of

universities was performed at this stage to investigate the role of engineering education in ASIC adoption.

1.1.6 Stage 6. Investigation of models.

Most of the reasons identified by users were found not to be based on fact, so the problem of identifying the real reasons for non-adoption became more difficult. In the systems sense, the problem became 'soft' or 'messy'. In stage six, several models were used to attempt to rationalise the system aspects of adoption and better understand the overall reasons for non-adoption. The models used have their roots in system, organisational and business research.

1.1.7 Stage 7. Investigation of technology transfer schemes.

The problem of ASIC adoption has been addressed by a number of national and international government initiatives. In stage seven, a number of such initiatives were reviewed in relation to the models that had earlier been identified. An international survey was performed in order to establish the extent of technology-transfer schemes outside of the UK.

1.1.8 Stage 8. Comparison with other industries

By this stage it had been established that there were some unusual problems associated with ASIC adoption, so a review of the Biotechnology industry was performed so as to ascertain whether the problems encountered in ASIC technology are also encountered in other high-technology industries.

1.1.9 Stage 9. Conclusions and recommendations.

In stage nine, all of the previous stages are brought together to form conclusions and make recommendations for appropriate action by industry, government and the SME base in order to improve the adoption of ASIC technology and enable UK companies to derive sustainable competitive advantage.

2. ASIC Technology and its history.

2.1 What is ASIC technology?

Application Specific Integrated Circuit (ASIC) technology is a family of related technologies which enable the production of low-cost integrated circuit solutions to electronic designs. The aim is to produce devices where the majority of the semiconductor processing stages that are performed during the manufacture of the chip are common to all users of the device-family, while the final few processing stages are specific to the particular application of one user.

Several well-known ASIC families exist, each of which has a number of variants. The basic families are shown in *Figure 2-1*. It is beyond the scope of this study to discuss the variants of each major group in any detail. The descriptions below are intended as an outline of the generic groups. Further details of the technologies involved may be found in a number of texts (Lee, 1990; Xilinx, 1994).

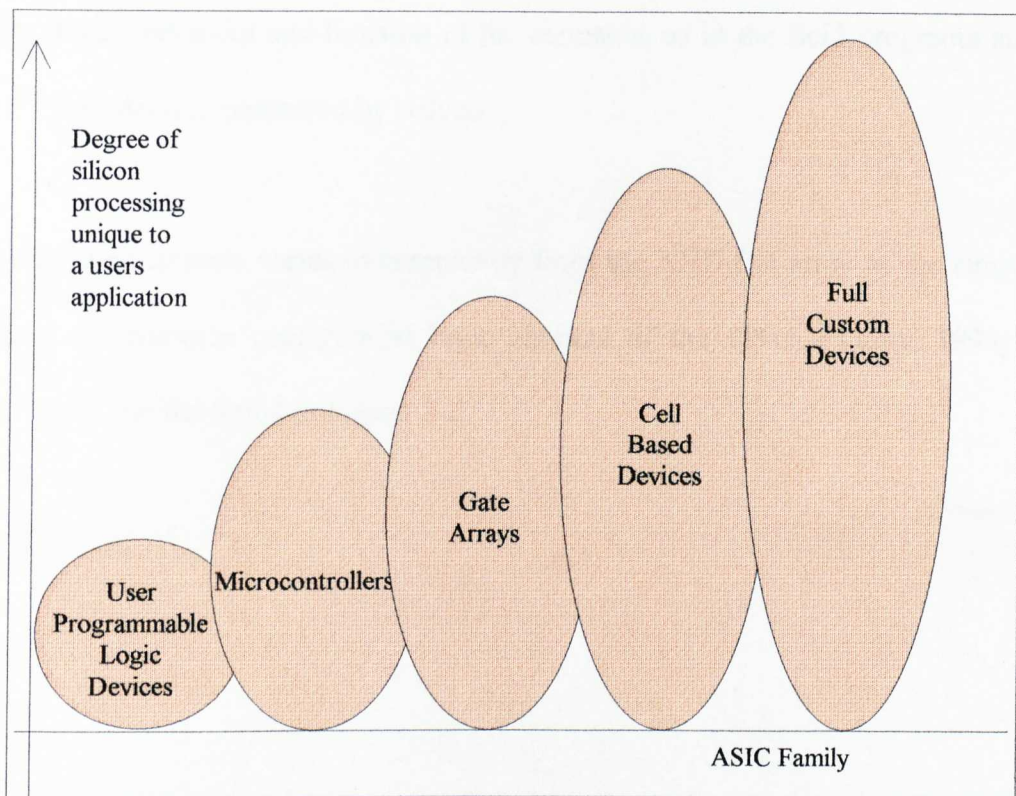


Figure 2-1. ASIC family of devices

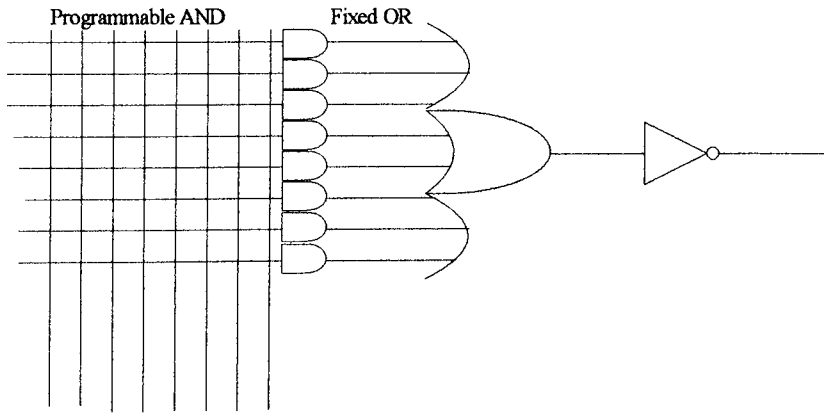
2.1.1 User-programmable logic devices.

These are considered, from the user viewpoint, to be the least complex of the ASIC families. An array of logic elements is fabricated on the chip, along with a means of connecting these elements which can be programmed by the application designer. Devices leaving the semiconductor manufacturer, while identical to each other, do not have any connectivity established between the logic elements. The customisation of the devices is done by the user.

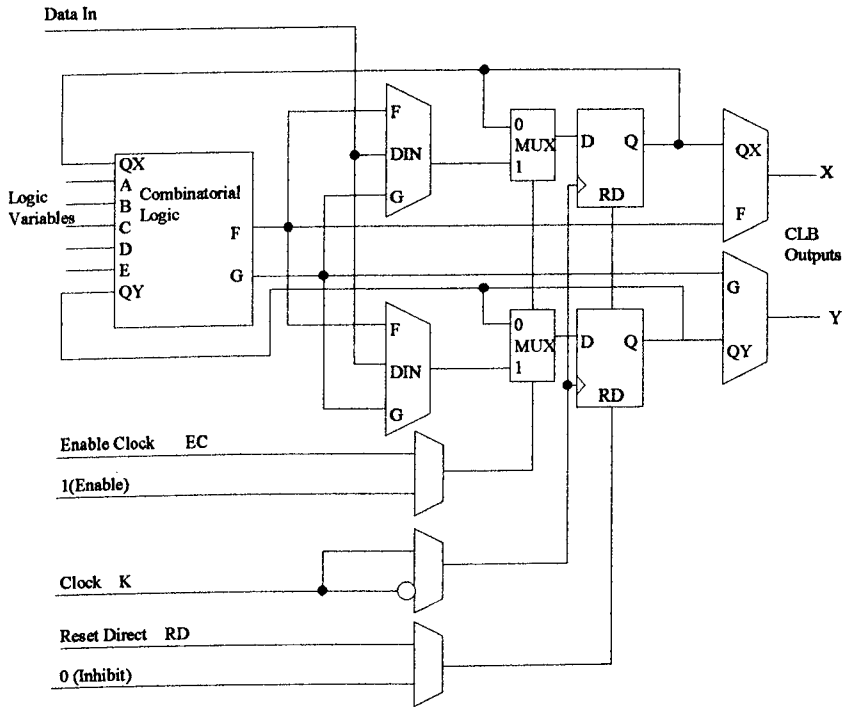
This customisation is performed in a variety of ways ranging from the blowing of fuses to leave only desired connections, as in Programmable Array Logic (PAL) devices, to loading a data pattern into Static Read-Only-Memory (SRAM) within the ASIC device which

governs the connectivity and function of the elements; as in the field programmable gate array (FPGA) devices pioneered by Xilinx.

The basic logic element varies in complexity from the AND-OR array of the simple PAL device to the complex configurable logic element of the FPGA (Xilinx, 1994; AMD, 1990). These are illustrated in *Figure 2-2*.



AND-OR Element of a PAL



A Xilinx Configurable Logic Block

Figure 2-2. Programmable device building blocks

2.1.2 *Microcontrollers.*

Often not considered to be ASICs, microcontrollers share many of the features of other ASIC families. In this case the common part of the chip is the microprocessor core. The function of the device is customised by its program, which is stored in the Read Only Memory (ROM) of the device. This programming is achieved either in the final photolithographic stages of the chip manufacture, or by the user programming PROM, EPROM, or flash-memory sections of the chip. Consequently, devices end up being unique to a particular application.

These devices can have remarkably low costs. Masked devices which have a non-recurring engineering (NRE) charge as low as £2,000 and a part cost of around 35 pence are not uncommon. This low cost has given them great popularity in the replacement of relatively simple logic circuits in addition to their more usual place in more sophisticated microprocessor systems used, for example, in control or computing applications.

In addition to the microprocessor core and program memory, microcontrollers can contain a number of on-chip peripherals including:

- Serial and parallel input/output devices
- Timers and counters
- A/D and D/A converters
- Additional non-volatile memory

2.1.3 *Gate-arrays.*

In a gate-array, the silicon vendor produces a base device consisting of an array of unconnected logic elements (typically 2-input NAND gates). To customise the device for

an individual application, the gates are connected using mainly metal interconnect during the final photolithographic stages of the manufacturing process. The devices may then be placed in a package suitable for the particular application. Such packages come in a variety of types and sizes with pin counts from less than 16 to over 300, and in packages suitable for both plated-through-hole (PTH) and surface-mount (SMT) manufacturing methods.

In this way, the function and packaging of the device can be customised to meet a particular user's application. As all of the manufacturing processes prior to the final metal interconnect layers are common to all designs, the base-wafers of uncommitted NAND gates are common to all designs and can consequently be manufactured in far greater quantities, and consequently lower cost, than would be the case for a unique chip. This architecture is shown graphically in *Figure 2-3*, which shows a channeled gate-array. With this technology, gates are fabricated in vertical diffusion-columns, with most of the metal interconnect passing over the blank wiring channels. A more recent variant of the technology does away with the wiring channels to produce a 'sea of gates' device in which the space previously occupied by wiring channels is filled with additional uncommitted gates. This allows a higher density of gates to be produced on the device, but adds to the complexity of the interconnect routing design, as passing a metal interconnect over a gate can render that gate unusable. Connection to the legs of the integrated circuit (IC) package are made using thin bond-wires between the I/O pad of the chip and the lead-frame of the package.

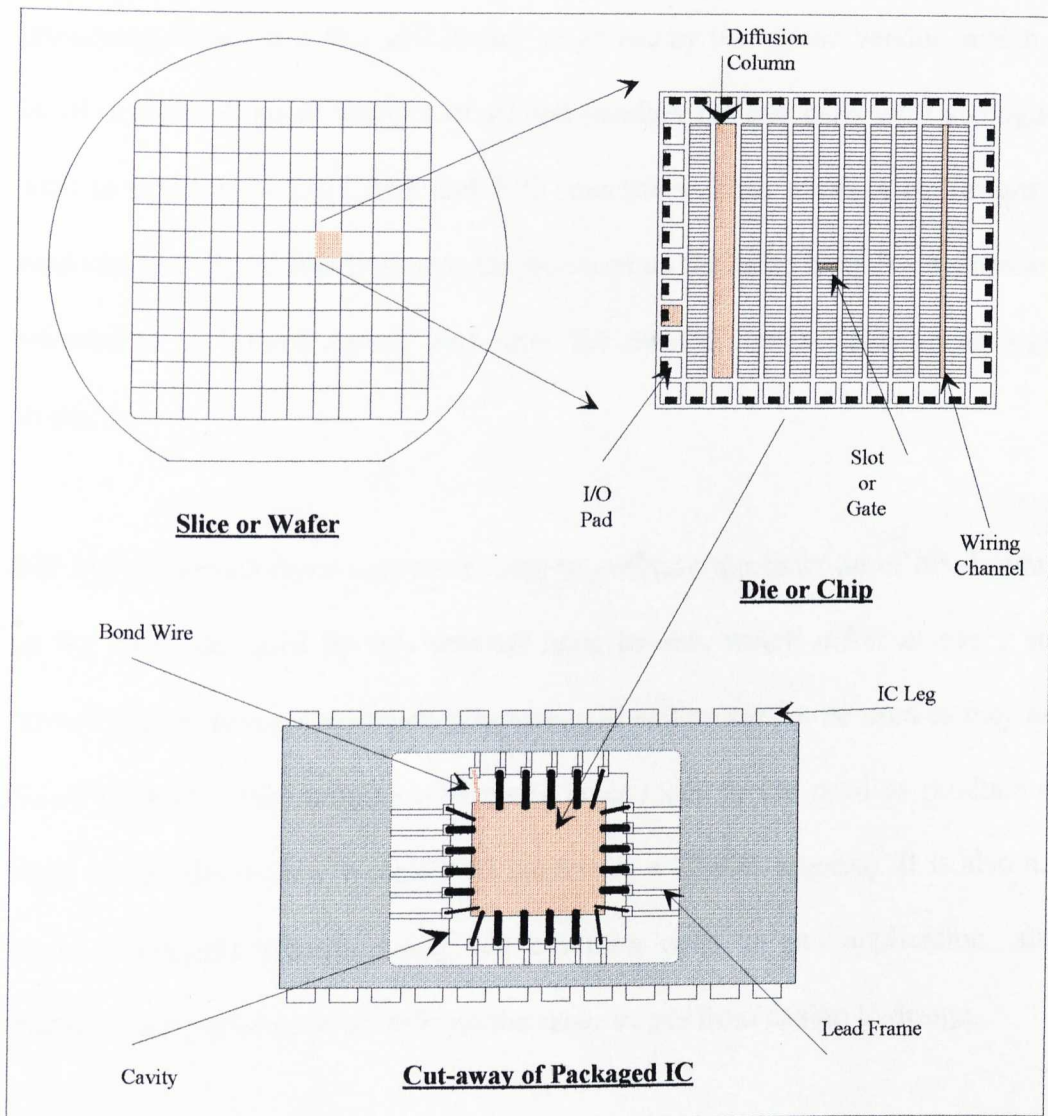


Figure 2-3. A channelled gate-array.

2.1.4 Cell-based (standard-cell) devices.

Cell-based devices take the degree of silicon customisation a stage further than array-based products. In cell-based devices a set of building blocks of different types of circuit elements are defined as cells. The cells come in a variety of types ranging from simple gates to more complex digital functions such as memory elements and may even include highly complex functions such as microprocessors. These cells are then designed as individual multi-layer entities which have individual layouts at each of the silicon

processing stages. It is this 'cell library' produced by the silicon vendor, which is common to all designs. A small number of silicon vendors include cells with analogue functions such as operational amplifiers and A/D converters. With these cells, designs using both analogue and digital functions may be produced on the same chip. Such chips are generally referred to as 'mixed signal' and form the most complex ASIC technology currently available.

The application designer uses these cells to generate the function of his design. However, as the chips designed by this process have layouts which differ at every stage of the manufacturing process, common pre-processed wafers cannot be used as they are in array-based products. This difference in every layer leads to the need to produce a complete mask-set for the device (typically 13 masks for a CMOS process). It is also necessary to have a complete manufacturing run common only to one application, although the manufacturing process itself follows the same stages from design to design.

These added levels of complexity in the design and tooling processes make cell-based devices more expensive than array-based devices at the design and prototype stages. The finished part may however be cheaper, as the ability to use precisely the building blocks best suited to the design generally leads to the design occupying a smaller silicon area than an equivalent array-based product.

The general layout of a cell-based chip is shown in *Figure 2-4*. A number of variants of the architecture shown in the diagram also exist, differing mainly in their ability to accommodate differently shaped cells.

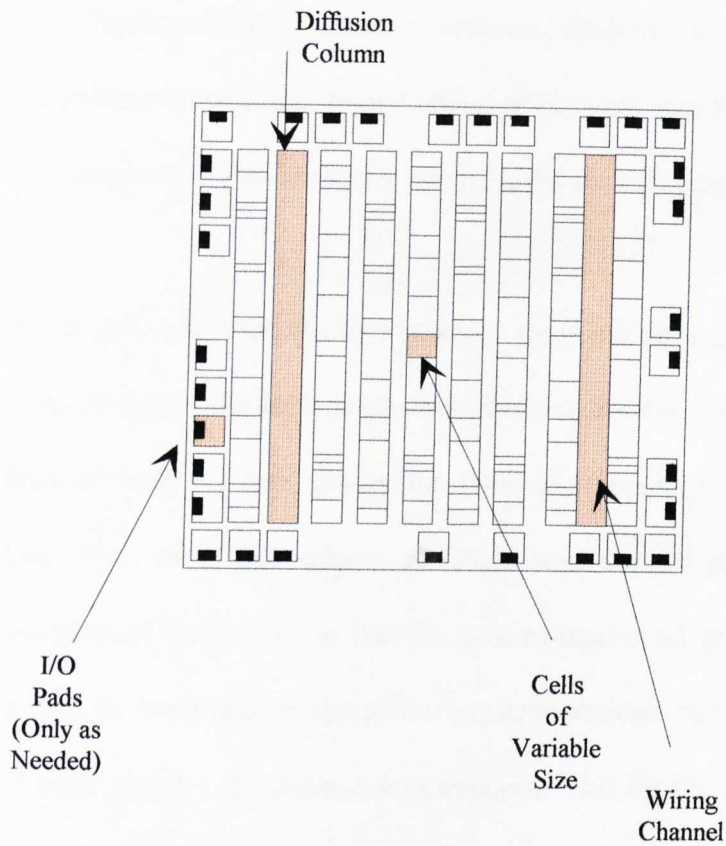


Figure 2-4. A column based standard-cell device

2.1.5 Full-custom devices.

The devices discussed so far are collectively referred to as 'semi-custom' devices. Full-custom devices are not generally considered as ASIC devices but are discussed here for completeness. They can be considered to be application-specific in only a minority of applications where very high volumes of manufacture justify the high cost of a bespoke design for an individual application.

In full-custom devices the design is constructed without the aid of a 'cell library'. Individual circuit elements such as transistors and resistors are used to produce the design. In this way maximum use is made of the silicon area, and device constructs most suitable to the application can be used rather than having to rely on those available in the cell

library. However, as there is little in common between designs, development costs are high, and problems associated with the unique layout of the chip may be experienced (e.g. cross-talk and noise problems which are rarely encountered in semi-custom designs).

Full-custom design is generally used for non-specific applications (e.g. microprocessors) and specific applications where the high production-volumes involved justify the extra risk and expense because of the lower final production costs of an optimally sized device (e.g. a video game). Even with such high-volume products, semi-custom processes are often used in the early versions of the product so that the time-to-market advantages of the semi-custom processes may be exploited. Full-custom implementations then follow when the volume of product sales justifies the extra design expense. This family of devices will be occasionally referred to later in this study, but is not specifically included in the research.

2.1.6 Hybrid ASIC types.

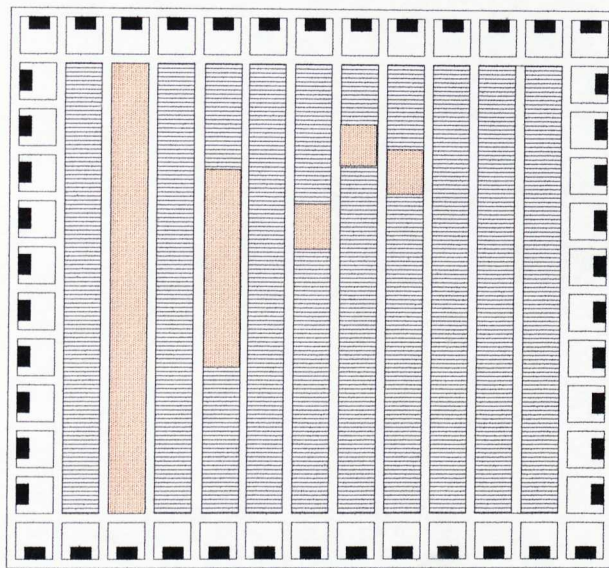
The types of device described in this chapter illustrate the basic techniques used in the fabrication of ASIC products. However, in order to overcome some of the inherent disadvantages of each of the approaches, some manufacturers have developed products which are best described as hybrids of the more normal techniques. Examples of such approaches include:

- **Hard macros:** In some applications the compact and predictable nature of standard-cells are mixed with the low design costs and versatility of gate-arrays. An example of this was a base-device developed by LSI Logic which contained four bit-slice microprocessor cells and an array of uncommitted gates. This allowed the bit-slice processors to be produced with the higher performance and smaller silicon area that can

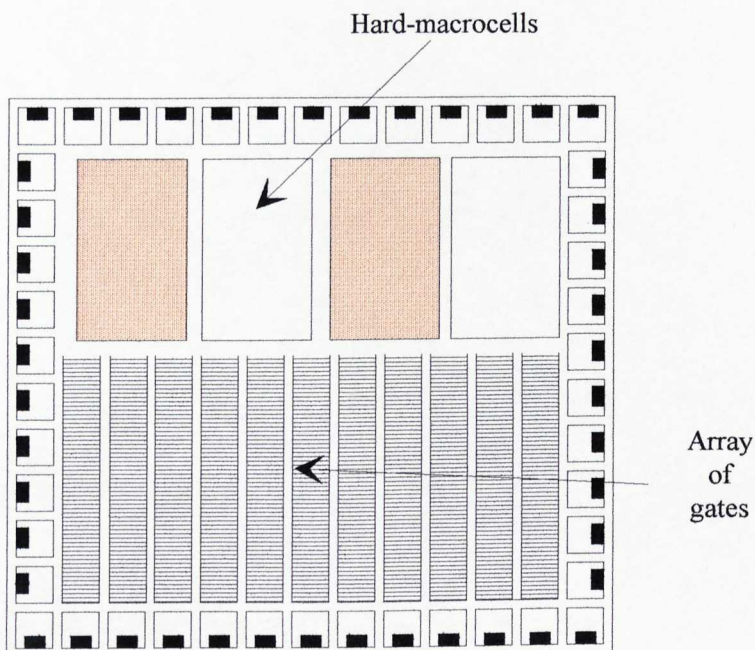
be achieved in a standard-cell, while the additional logic could be fabricated in a gate-array technology with its inherently lower cost.

- **Soft macros:** In order to overcome the need to re-invent complex cells in gate-array designs, some manufacturers produce ‘soft macros’. These are pre-designed complex elements (for example the bit-slice microprocessor mentioned above) which are made available to gate-array designers as net-lists or hardware design language (HDL) representations. These are different to standard-cells in that their layout is not fixed, so they will occupy different silicon areas to fit-in with a design each time they are used.

Figure 2-5 shows how these two approaches differ in the design of a chip containing two bit-slice microprocessors.



Soft macros distributed over chip to suit layout



Two of four available cells used

Figure 2-5 Hard and soft macrocells

In the upper example in *Figure 2-5* the desired microprocessors have been incorporated into the design, fitting in with the rest of the design as dictated by the layout tool. In the lower example, a base-device containing four hard-macrocell processors has been used. As the design only requires two such devices, two remain unused. This illustrates the major

problem with this approach; the silicon vendor has to predict the most universally useful combinations of macrocells, and will seldom be correct in his choice. The advantage is that the resultant cell will have a layout and hence performance which is consistent across multiple cells. The soft-macro will not, as performance is significantly affected by layout.

2.2 A brief history of ASIC technology.

As with most areas of technology, the history of ASIC technology has a direct influence on the way that it is perceived and used in the present. For the purposes of this study, the history of the ASIC device also needs to be considered in relation to a number of other technological and business developments that occurred in the electronics industry in the post-war period. This brief history will consider some of the principal developments between 1960 and the present, and is summarised in *Figure 2-6*.

The decades shown in the diagram refer to the time at which the technologies became widely available to the semiconductor user rather than the point at which they were invented or developed as a number of technologies, including Complementary Metal-Oxide-Semiconductor (CMOS), remained unexploited for a considerable length of time after their invention.

Semiconductor Technology	DTL Sylvania TTL	74 series TTL	4000 CMOS	Advanced TTLs	HCMOS CMOS Memory	One micron CMOS	0.5 micron CMOS	3.3V CMOS
Masked ASIC Technology				ULAs 100 Gates	CMOS arrays 10k gates	CMOS arrays 100k gates	CMOS arrays 1M gates	CMOS arrays 5M gates
Programmable ASIC Technology				MMI PAL	First FPGA (Xilinx)	Antifuse FPGA	25k gate FPGA	100k gate FPGA
Microcontroller Technology			Intel 4004	16-bit devices	32 bit microcontrollers devices (on-chip peripherals)		Complex on-chip peripherals & DSPs	
Business Developments		Mostek formed		Formation of Inmos	ASIC companies e.g. LSI Logic		Design consultancies	
Design Tools					Logic simulation	Schematic capture	Logic synthesis	Mixed signal simulation
	1960s	1970s	1980s	1990s				

Figure 2-6. Technology roadmap since 1960.

In 1952, Dummer heralded the practical use of the integrated circuit (IC) when he said, “It seems now possible to envisage electronic equipment in a solid block with no wires” (Lee, 1990), but it was not until the 1960s that the integrated-circuit became commercially available in any quantity. ICs were originally developed by companies such as Texas Instruments and Fairchild to reduce the weight and increase the reliability of electronics in spacecraft and airborne weapons systems. However, with few exceptions, general electronics companies were restricted in their use of ICs to the standard products produced by the semiconductor companies.

These standard products began in the 60s with small scale integration (SSI) components (e.g. NAND gates and latches) fabricated in technologies such as Diode-Transistor Logic (DTL). By the 1970s the number of devices that could reliably be manufactured on a single chip had increased and medium scale integration (MSI) components (e.g. counters and multiplexers) were available. By this time, fabrication technology had moved on to Transistor-Transistor Logic (TTL) and 4000 series CMOS (Lavington, 1976; McLean & Rowland, 1985; Morris, 1990). TTL had been originally developed by Sylvania in the mid 60s, but it did not increase significantly in popularity until the launch of the 74 series TTL by Texas Instruments in the late 60s (Horowitz & Hill, 1995)

Large scale integration (LSI) began with the introduction of the microprocessor and integrated memory devices in the early to mid-seventies. It was at about this time that semiconductor companies began to develop devices in which an array of logic-gates were fabricated on a chip, leaving the final layers of metal interconnect to be defined by the user. By the late seventies a number of semiconductor companies including Plessey, Ferranti and Fairchild had produced Uncommitted Logic Array (ULA) devices, which

contained about 100 gates per chip, and were beginning to see applications in commercial systems such as the ICL 2900 and IBM 360 mainframe computers and other high-speed computing systems (Gosling, Kinniment & Edwards, 1979).

Meanwhile, a revolution in the business aspects of the semiconductor industry was occurring, predominantly in the USA. It was becoming normal for bright groups of engineers from the major semiconductor vendors to leave their employers to form new, small semiconductor-companies. Silicon Valley was becoming important and the US semiconductor industry was gaining a massive technical and commercial lead over the rest of the world. Two such entrepreneurial engineers were Richard Peritz and Richard Hanschan who, having been involved in the successful development of the 74 series TTL for Texas Instruments, left to set up Mostek, a company which was to hasten the development of Metal-oxide-semiconductor (MOS) and CosMOS (later to become CMOS) technology. Peritz was later to be instrumental in the formation of Inmos in the UK in conjunction with Ian Barron. The significance of this company with regard to the UK microelectronics industry and government intervention in technology transfer will be discussed later.

CMOS quickly became established as a major process-technology due to its small feature size (the size of the smallest feature that could be fabricated on the silicon surface), and low power-consumption which allowed complex devices to be fabricated without the thermal problems previously associated with LSI devices based on other MOS or bipolar technologies. In Silicon Valley, a small number of companies were combining the advantages of CMOS with those of ULAs to produce families of CMOS gate-arrays. One such company was LSI Logic, which was to grow to dominate the world ASIC market and

remains important in that market today.

Advances in CMOS technology came to be driven by the need for ever denser memory devices for the computer industry which was growing rapidly during the 1980s. This drove down the geometry of the patterns etched on the silicon surface (the feature size), from the 5 microns that was common at the start of the decade to the sub-micron technologies available today (0.5 micron is commonly available at the time of writing). As these denser technologies became available to gate-array manufacturers, economically viable gate-array devices progressed from having a few hundred gates available to the designer, to today's situation, where gate-arrays containing over one million gates will soon be commonplace. The need for lower power-consumption to meet the needs of battery-powered equipment also led to the development of devices operating from a 3.3 Volt power supply rather than the more traditional 5 Volts.

Programmable logic devices were also developing during this period. In the mid 70s Monolithic Memory Inc.(MMI) launched the Programmable Array Logic (PAL) device. Based on fuse PROM technology, these devices had a programmable AND/fixed OR configuration (*Figure 2-2*). The early devices had eight 'sum of product' terms and up to eight latches. They had a maximum of around sixteen inputs/output (IO) pins. Propagation delays through the combinatorial path were around 35ns. Early implementations required the connectivity to be manually calculated and described in binary notation as a 'fuse map', but a design-entry language (PALASM) was soon developed which could automatically formulate a fuse-map and device blowing information from a set of Boolean expressions. By the early 80s these devices were becoming commercially accepted and used in large volumes in products such as the Honeywell DRTI real-time digital control

system, and later in the Microdata 'Spirit 1' range of multi-user minicomputers.

During the 80s the complexity and speed of programmable logic devices developed, and a number of new technologies emerged which came to rival the mask-programmed gate-array in cost and performance at gate-counts of up to about 10,000 gates. The market moved fast, along with other semiconductor technologies. Xilinx, for example, was formed in 1984 and released the first CMOS SRAM based FPGA a year later. In the years to 1990 they maintained a 40% per year improvement in speed, a 52% per year increase in density, and a 46% per year decrease in silicon cost. (Xilinx,1993). In 1994, Xilinx offered, at the top of its range, the XC4025, a 25,000 gate-equivalent device with gate delays of the order of a few nanoseconds. By mid 1995, a number of manufacturers were claiming a 50,000 gate device, and early in 1996 some were announcing devices with 100,000 gates (Bursky, 1995). However, in all of these cases it should be remembered that the maximum utilisation of gates in programmable devices may be as low as 40%, so reducing the effective gate-count. Competing technologies emerged using different device-configuration methods. One such method was the Actel 'Antifuse' system in which internal device connections are made through antifuses which become low-impedance when a large programming current is passed through them (so named because this is the opposite effect to that encountered in a fuse which goes open-circuit on the application of a high current).

Also important to the development of ASIC technology was the emergence of new and innovative design tools. While in the days of 100 gate devices it was possible for a single design-engineer to design a chip at transistor level using well established, paper-based design methods, and get the design correct, this quickly became impossible as the gate-

count rose. In order to make the higher density technology usable, computer aided design (CAD) tools started to appear. Commercial systems were available in the late 1970s. These were either developed by the ASIC companies (e.g. LSI Logic's 'LDS' simulation tools), or were general purpose tools that could be easily adapted to fit many vendors' devices. Three US companies quickly came to dominate this market (Daisy, now Veribest; Mentor; and Valid, now merged with Cadence). The functionality of these tools has developed over the years, with text entry of circuit netlists giving way to schematic entry where computer based drawing tools could be used to draw circuits using the symbols familiar to engineers. More recently, hardware description languages (HDLs) and logic synthesis have become more widely used. Using these tools the final circuit is produced automatically by a software system driven by a description of the behaviour of the system written by the designer. Mixed-signal tools have also become available which allow both the analogue and digital parts of a circuit to be simulated concurrently.

Another development, which is important when considering technology adoption, is the migration of design tools from the mainframe and high-cost workstation platforms normal in the 80s to the easily available Personal Computer (PC) platform. This migration has taken place as the power of the PC has increased. At the time of writing, CAE systems capable of developing all of the ASIC technologies discussed here, with the possible exception of very large masked devices, are commonly available at relatively low cost on PC platforms. This trend is discussed in more detail in *Chapter 7*. Another trend influencing SME adoption is that the user-interfaces of the CAE tools became more user-friendly as time went on, so the amount of time necessary to become familiar with the use of the tools reduced. In the early 1980s it was not uncommon for a new user of CAE tools to require several weeks training in their use. At the time of writing it is unusual for such

initial training to take more than a few days.

Developments in devices based on logic elements were matched in processor-based chips. The first commercially available microprocessor device was probably the Intel 4004 which went on the market in 1971. Texas Instruments claim to have demonstrated a device a year earlier, but it was not patented until 1971. These 4-bit devices (4-bit here refers to the width of the ALU; i.e. the device would have a 4-bit adder) were microprocessors rather than microcontrollers, because they did not have any program holding memory or any other peripheral device incorporated in the chip. Microprocessors containing ROM to store program information began to appear in the late 1970s and were in general use in the early 1980s. These became known as microcontrollers due to their suitability for simple control applications. During the 1980s, the complexity of microcontrollers rose in step with developments in the industry at large. Feature size was reducing and the adoption of CMOS was becoming commonplace. Eight, sixteen and thirty-two bit devices appeared, and complex peripheral devices were incorporated into the chips (e.g. UARTs, A/D converters). These developments were also supported by the emergence of design tools for software development that enabled significant simplification of the software design task. These tools include advanced compilers and Computer Aided Software Engineering (CASE) tools. As with the CAE tools discussed earlier, most of these sophisticated tools became available on low-cost PC based platforms.

It can be seen from the above that all of the ASIC families are continually increasing in complexity. It can also be shown that such complexity is developing at an ever increasing rate. This is common in the semiconductor industry and is best summarised by the rate of development of the Dynamic Random Access Memory (DRAM). This is often regarded as

the driving technology for the industry, as its increasing density and ever smaller feature-size allows development of denser devices in all of the other semiconductor families. This in itself has led to lower-cost processors becoming available in PCs which has increased the sophistication of design tool available to the SME based electronic designer. The history of this increase in DRAM density is shown in *Figure 2-7*, and is clearly logarithmic. The diagram is derived from the point in time at which the author was designing a particular size of chip into commercial products and so represents the time at which each device size became commercially viable.

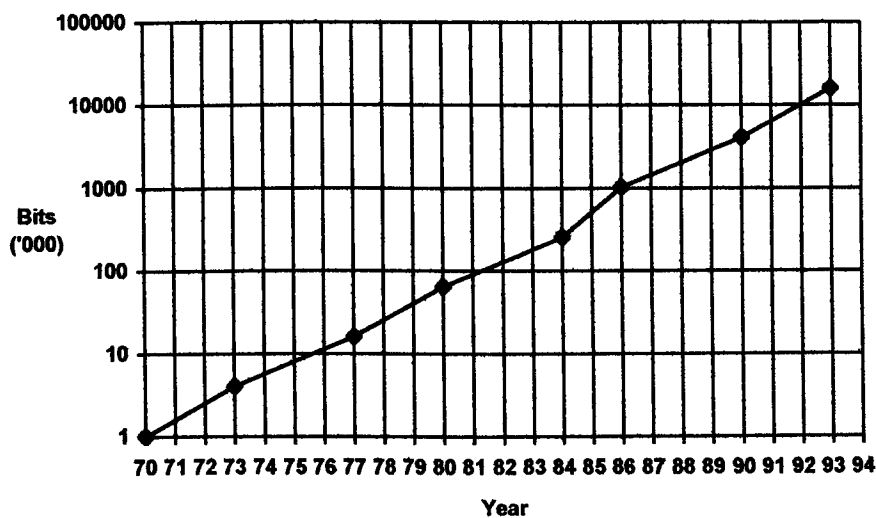


Figure 2-7. DRAM density over time

2.3 Experience curves describing ASIC technology development.

The development of microelectronic technology over time can be portrayed as a set of experience curves. The simplest indication can be derived by plotting unit cost against time, but this is itself difficult to determine (Abell & Hammond, 1979). A useful analogy to experience that may be used to analyse experience in ASIC developments is gate-count, which is itself analogous to DRAM device-density as it is this process-density that is the technology driver of gate-density and consequently unit cost of all ASIC technologies. The derived curve for DRAM density, and by analogy ASIC device experience, is shown in *Figure 2-8*.

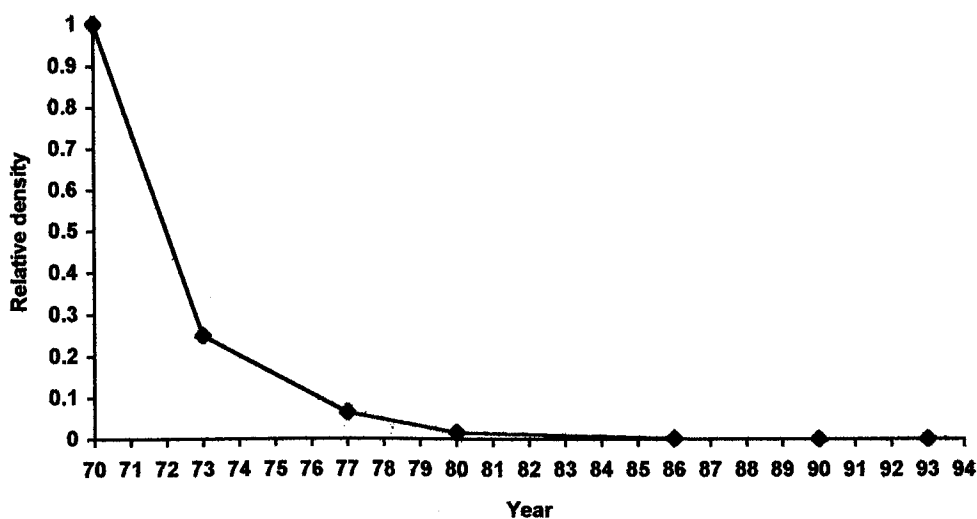


Figure 2-8. DRAM manufacturing experience curve

The experience effect is generally considered to stem from a number of sources (Abell & Hammond, 1979). These sources are discussed below.

2.3.1 New production processes and getting better performance from production equipment.

This is probably the most important factor in relation to microelectronic technology. New processes and equipment are continually being developed which allow both larger wafers to be produced, and the size of features on the chip to be reduced while maintaining acceptable production yields. These production processes are normally introduced in DRAM production, but quickly migrate to other technologies, including all of the ASIC technologies. In addition to the introduction of new and better equipment, most fabrication facilities operate continuous yield improvement programmes which enhance the yield from existing equipment.

2.3.2 Product standardisation

Product standardisation has occurred in a number of major areas. For example, pin-out, package type and the access algorithm for some devices have been standardised between manufacturers. For example, The Joint Electronic Device Engineering Council (JEDEC) has standardised a number of formats for the transfer of programming information for programmable logic, the physical dimensions of chip packages, and the test interface for many microelectronic circuits (the JTAG methodology). Some standardisation of interfaces between designers and manufacturers has also taken place; for example with Verilog or VHDL netlist standards, or GDSII as an interface standard for chip layout information. This standardisation is helpful to the SME engineer as it reduces the amount of training necessary before starting to design in a particular technology, and can make the

migration of design from one technology to another more straightforward (e.g. by initially designing in VHDL, migration to a masked technology can be simplified)

2.3.3 Product redesign

When smaller device-geometries become commercially available in a particular processing technology, ASIC families based on that technology are soon redesigned to exploit the additional features of the smaller geometry (e.g. higher speed, lower power). In addition, some changes specific to ASIC technology have also occurred from time to time which have led to radical changes in internal architecture. One example of this was the advent of 'Sea of Gates' technologies in which routing channels in gate-arrays are replaced by additional gates allowing higher silicon utilisation but requiring more complex routing algorithms. This results in a lower overall cost for a particular chip and so reduces the cost of entry to the technology for the SME adopter. The increased complexity of routing algorithm has little effect on the SME adopter, as device layout is generally performed by the silicon vendor.

2.3.4 Labour efficiency & de-skilling

The labour content of ASIC production is small in comparison with the capital invested in production equipment. A 'state of the art' IC production facility is generally considered to cost in the region of a billion dollars. Consequently, labour efficiency in production can only have a minimal effect. However, some labour efficiency savings have been made in other areas. For example, sales and marketing of the more 'commodity' ASIC devices (e.g. FPGAs and microcontrollers) has largely been transferred to distribution rather than direct sales.

2.3.5 Other implications of the experience curve. Moore's Law.

David Manners (Manners, 1996) uses market statistics from Dataquest and ICE to derive the cost/price curve shown in *Figure 2-9*.

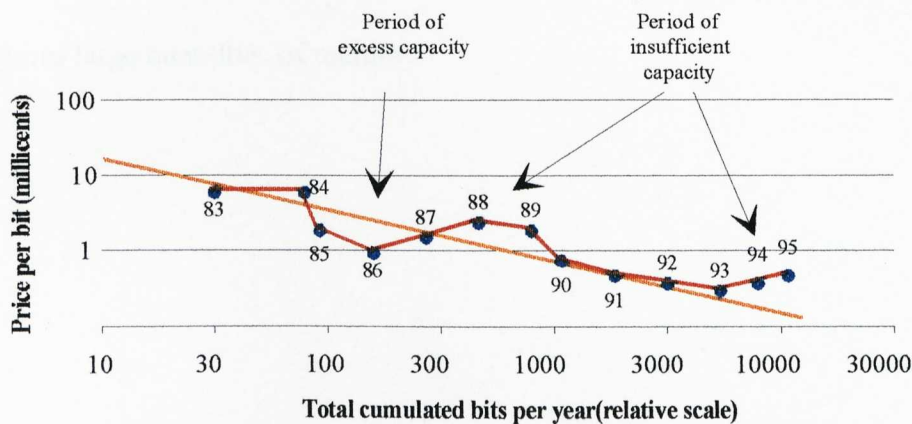


Figure 2-9 DRAM price vs cost

The straight line represents the experience curve known to exist in the semiconductor industry. In essence, the cost of a given area of processed silicon remains fairly constant, while the number of components on it doubles approximately every 18 months. This has become known as 'Moore's Law' after the founder of Intel, who first expressed it. Under normal circumstances, the price of a given semiconductor product would be expected to follow this experience curve.

However, market conditions also have a bearing on the price. Between 1993 and 1995, as in 1988/89, demand for ICs exceeded supply, and a firming of price resulted. The indication from the trends shown in *Figure 2-9* is that once this supply problem has been relieved (by the large number of new plants coming on-stream in the near future) a dramatic price reduction will ensue. Such price reductions have previously resulted in

booms in the sales of technology dependent products (e.g. personal computers) as their relative prices fell. This has to be good news for the potential user of these technologies, as such price reductions will inevitably lead to similar price reductions in ASIC devices using the same base technology. The first signs of this price reduction were seen in mid 1996, and continued into 1997. This is predicted to herald the introduction of digital television which requires large quantities of memory.

2.4 Family tree of available technologies.

As a result of these developments we come to today's position where a wide variety of ASIC devices exist to meet the needs of all sectors of the electronics industry, from the low-volume to the high-volume manufacturer, and from simple low added-value products to complex state of the art computing and communication devices. The family tree of currently available devices is shown in *Figure 2-10*.

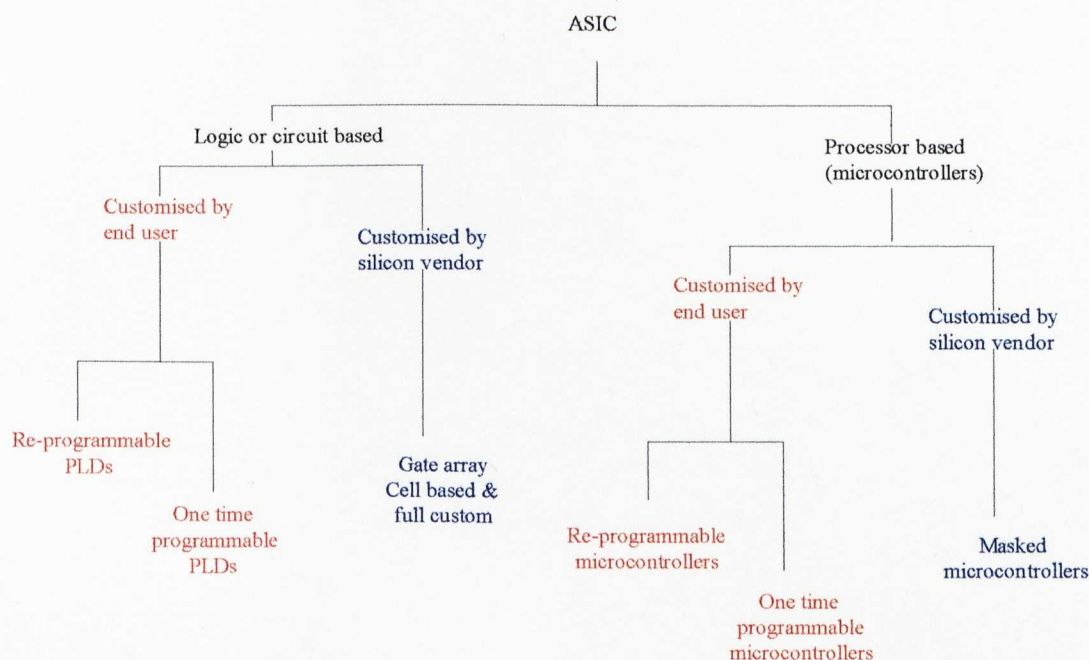


Figure 2-10 *The ASIC family tree.*

This family tree delineates ASIC families by the basic architecture of the devices and the method used to customise them. ASIC devices are either based around processors, and programmed using computer programming languages, or are based around logic or circuit elements (e.g. gates, latches, amplifiers). In both cases a fairly similar set of customisation technologies can be used, ranging from mask customisation by a silicon vendor to user

programmability that may be performed once only or many times using reprogrammable devices. Many similarities exist between the processor and logic-based devices which prevent separate treatment of the two types as was the case in the past, when only masked devices were claimed as ASIC. This strange differentiation between masked and non-masked technologies has cost the industry dear, causing many potential ASIC users to shy away from the technology as they considered all ASIC technologies to be difficult and risky (McArdle, 1995). This is one of the misconceptions that must be overcome if the adoption of these technologies is to be encouraged.

2.5 Relationship of technology to manufacturing methods

It is interesting to relate the different ASIC technologies and customisation methods shown above to standard methods of production flow management. Methods of production flow management can be considered in relation to production volume as shown in *Figure 2-11*.

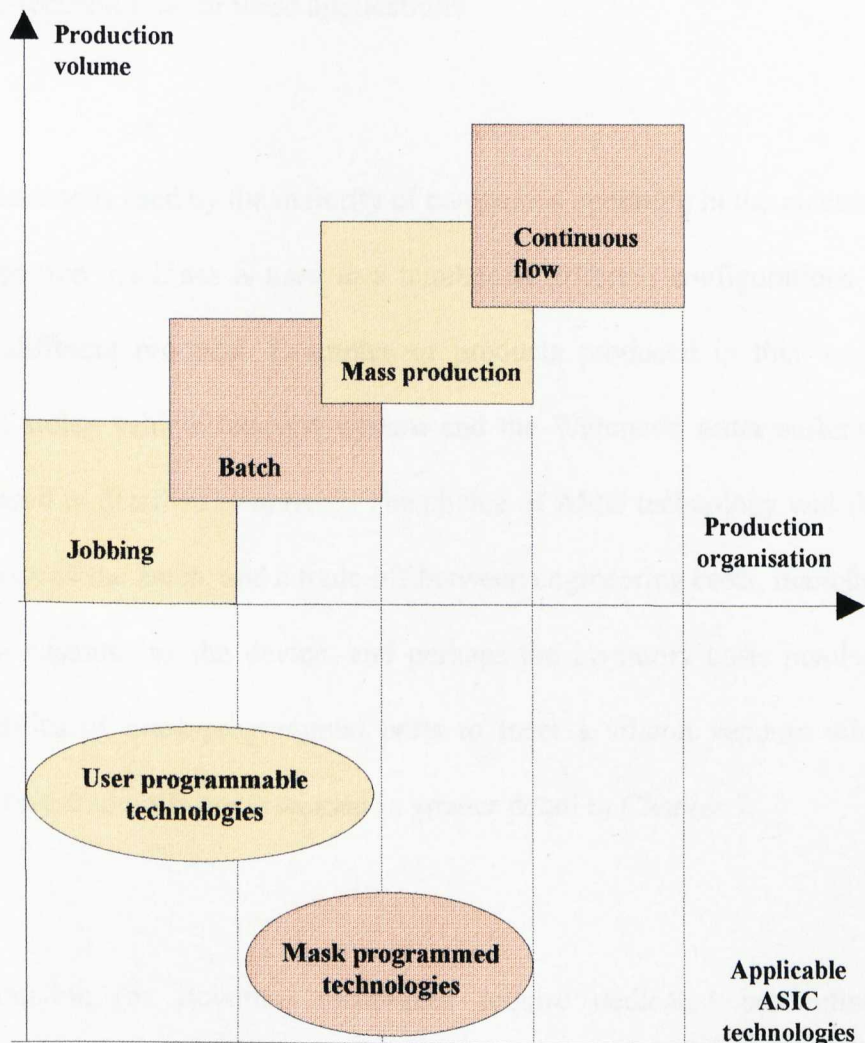


Figure 2-11 *Production organisation and ASIC technology related to volume.*

Jobbing production involves the manufacture of single or small numbers of individual items, and generally uses a highly skilled workforce to produce such individual items.

Examples of products requiring jobbing manufacture in the electronics sector include technology demonstrators (e.g. the Ionica Link Equipment discussed in *Chapter 3*) or equipment where each delivered product is a variant of a basic design (e.g. HJ Weir's laundry folding equipment discussed in *Chapter 3*). Clearly, in terms of ASIC technology, low design costs, low NRE, and ease of change are important in this process. Consequently, programmable logic and non-masked microcontrollers are the most appropriate technologies for these applications.

Batch production is used by the majority of companies operating in the electronic sector. A set of production machines is used in a number of different configurations to produce a variety of different products. Examples of products produced in this way include the TRACKER stolen vehicle recovery system and the Waterside water softener, which are both discussed in detail in *Chapter 3*. The choice of ASIC technology will depend on the economic size of the batch, and a trade-off between engineering costs, manufacturing costs involved in customising the device, and perhaps the inventory costs involved in buying large quantities of mask-programmed parts to meet a silicon vendors minimum order quantity. These trade-offs are discussed in greater detail in *Chapter 7*.

Mass production (or flowline) techniques require dedicated production lines and equipment to be used for the manufacture of a single product. Few electronic products can be considered to fall into this category, particularly those of SMEs. Electronic products that do fall into this category include radio pagers and mobile telephones. In these cases mask-programmed technologies become most attractive. They have the lowest cost in

high-volume, and their development and NRE costs can be more easily amortised over the higher manufactured volume.

Continuous flow, included here for completeness, is generally associated with chemical rather than mechanical or electronic manufacture. It is difficult to conceive of any electronic product that might be considered in this context.

3. The structure of the UK manufacturing base.

In recent years, there has been growing interest from both academic and government bodies in the role of the Small and Medium Enterprise (SME) in all sectors of business. This increased interest can only be justified if such companies can be shown to have a significant impact on the economy.

3.1 Size of the UK manufacturing base

There is considerable difference in opinion as to what constitutes a small or medium sized enterprise. A variety of definitions exist based on such criteria as the number of employees, turnover, ownership and asset size. In an attempt to overcome these difficulties, the European Commission has defined the following terms which are becoming standard in research concerned with company size (Storey, 1994):-

Micro enterprises	Those between 1 and 9 employees
Small enterprises	Those between 10 and 99 employees
Medium enterprises	Those between 100 and 499 employees
Large enterprises	Those over 500 employees

Table 3-1. Enterprise size definitions

The SME sector is consequently considered to be enterprises (with some exceptions such as agriculture) that employ fewer than 500 workers. In the UK, the Department of Trade

and Industry (DTI) generally reduces this figure to 250. Additional definitions, often based on turn-over, are also sometimes applied.

There is no definitive data available on the size and breakdown of the SME sector in the UK but a number of indicators can be used to estimate this breakdown, including VAT registration (although not all SMEs are VAT registered), and company registrations (although a large number of registered companies have ceased trading or never traded). A translation matrix produced by Graham Bannock & Partners is then used to translate turnover to likely employee numbers to give what the DTI believe to be the most accurate estimate of SME breakdown for the UK (Storey, 1994). It is difficult to believe that such vague figures are used as the basis of industrial policy which is so important both nationally and in the context of the European Community. However, the interpolated statistics suggest the breakdown shown in *Table 3-2*.

Employment size band	Number of companies (‘000)			Percentage of all businesses			Percentage of total UK employment in these businesses		
	1979	1986	1991	1979	1986	1991	1979	1986	1991
1-2	1099	1595	1735	61	64	64	7	11	11
3-5	319	535	565	18	22	21	6	10	10
6-10	179	178	196	10	7	7	7	7	7
11-19	109	84	97	6	3	4	8	6	6
20-49	46	56	65	3	2	2	7	8	9
50-99	16	16	20	1	1	1	5	6	7
100-199	15	9	10	1	-	1	10	7	8
200-499	5	5	6	-	-	-	8	10	9
500-999	2	2	2	-	-	-	8	7	6
1000+	2	1	1	-	-	-	35	29	27
Total	1791	2481	2697	100	100	100	100	100	100

Table 3-2. Breakdown of UK businesses by size.

The likely inference from these statistics, which needs to be treated with some caution, is that the number of small companies in the UK increased in the 80s and continues to increase in the 90s, with much of the growth being in the micro-enterprise sector. However, although SME companies account for over 90% of the UK company base, they employ only 28% of the employee total.

The position is not significantly different in Europe, as can be seen in *Table 3-3*. Here, the breakdown shows that over 99% of manufacturing enterprises are micro or SME in size and that manufacturing enterprises represent around 14% of the total number of companies (Levy, 1994).

	No of enterprises	Number of employees			
		Micro	Small	Medium	Large
		%	%	%	%
Total	13,500,000	91.3	8.0	0.6	0.1
Manufacturing	1,900,900	82.7	15.1	1.8	0.4

Table 3-3. Employment in the EU.

If these figures are extrapolated for UK companies, it would suggest that over three hundred thousand companies of the 2.7 million companies registered in the UK could be considered to be manufacturing enterprises. If as little as 5% of these could use electronics in their products, and each only produces one product, then there should be a potential for in excess of 15,000 separate ASIC implementations.

In order to verify the validity of these figures it is useful to approach them from a different direction. DTI figures suggest that the UK has over 9500 companies in its electronic manufacturing sector (SBA, 1996). This does not include companies in sectors that could use electronics but do not (e.g. electro-mechanical companies, industrial control companies, toy companies) so it is not out of the question to suggest that at least an equal

number of companies could use microelectronic technology. This leads to a possible market base of around 19,000 companies; a figure not dissimilar to the 15,000 calculated using the first method of approximation. In reality, the potential market is probably considerably higher than this as most of these companies are likely to have more than a single product in their portfolio.

It can be seen from this that the potential market for ASIC use by SMEs in the UK and Europe is large. The examples discussed later in this chapter show that SMEs can make significant and successful products using ASIC technology. It can be shown that any product that does or could use electronics in its construction may benefit from the use of ASIC technology. The supposition remains however that UK SMEs are not taking advantage of this technology and may fall behind overseas competitors that do. Research undertaken for this study has shown that perhaps as few as 20 masked ASIC and around 200 programmable ASIC based products are developed for or by SME manufacturing companies in any single year. The question is, “ Why is this the case?”. This study identifies the reasons and investigates ways in which the uptake of the technology might be improved.

3.2 The changing structure of manufacturing businesses.

While considering the case-studies of the successful adoption of ASIC technology that appear later in this chapter, it is useful to review the structure of manufacturing businesses so as to consider whether a particular organisational structure can have any effect on a company's ability to adopt new technologies such as microelectronics.

The traditional view of a company structure is shown in *Figure 3-1*. Traditional, and particularly large companies, have tended to adopt this structure and attempted to grow or acquire all of the skills necessary to fulfill each of the functions (Richards, 1991).

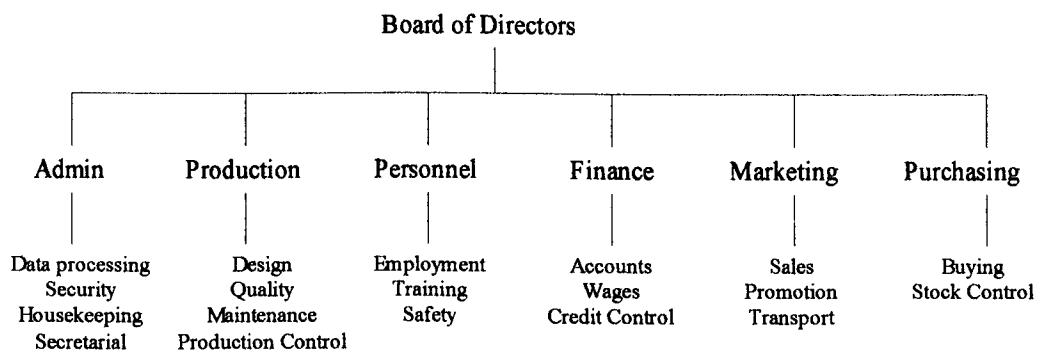


Figure 3-1. Traditional company structure

However, this rigid and often inflexible structure is being replaced by far more relaxed structures where a company no-longer feels that it needs to retain all of the skills necessary to its success in in-house teams. Initially this led to a degree of out-sourcing of some functions (e.g. transport, cleaning) but increasingly it is leading to the establishment of product based companies that are simply the hub of a 'skill-network' (Peters, 1992). Peters quotes a number of large corporations who are now firmly committed to out-sourcing major parts of the primary as well as the secondary components of their businesses. Such

companies include General Motors, Ford, General Dynamics, McDonnell Douglas and MCI.

In the extreme, this leads to a company at the centre of a hub which is little more than a 'brand owner'. The company is able to closely follow the needs of its customers by being continually adaptive, and sourcing all of the components of its business from 'best in class' suppliers. This is illustrated in *Figure 3-2*.

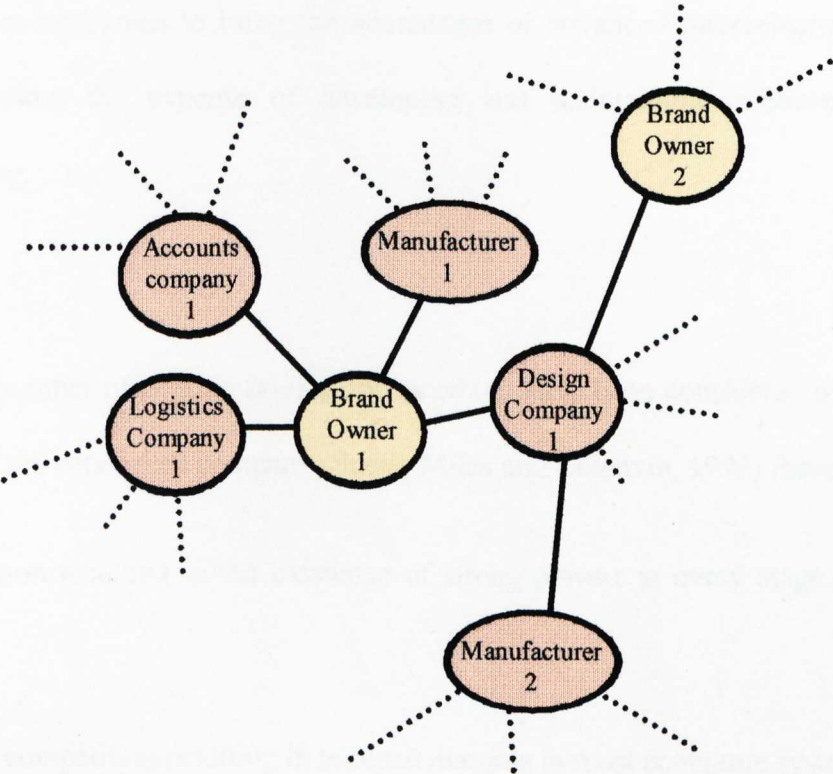


Figure 3-2. *A networked company.*

The brand-owning company (brand-owner 1) has chosen to out-source most of its operational components with the exception of sales and marketing. In doing so it forms a network with the supplier companies shown in the diagram. However, it does not have exclusive use of these suppliers. In the example shown it shares a design company with another brand-holder. These are loose relationships that can be changed to suit the

changing needs of products and markets, and so allow a company to concentrate on a small number of core competences, and the development and protection of its individual brand.

It is interesting to note that all of the companies discussed in the case-study section of this chapter are network organisations of the type described here. To a greater or lesser extent, each out-sources major parts of its primary function. In all cases both the design and the manufacture of at least the electronic parts of their products are out-sourced. This has allowed these companies to bring the advantages of advanced microelectronics to their products without the expense of developing and maintaining in-house design and manufacturing.

There are a number of generic driving forces which have been considered to promote the formation of the networked company (Snow, Miles and Coleman, 1993) these include:

- Globalisation resulting in the existence of strong players at every stage of the value-chain
- Increased competition resulting in reduced margins in most economic systems
- Technological change resulting in shorter product life-cycles and lower entry barriers

All of these forces can clearly be seen to be operating in many of the markets in which microelectronics operate, and in all of the markets identified in the case studies discussed later in this chapter.

There can however be some disadvantages in out-sourcing primary functions which should be considered (Peters, 1992). These are said to include:

- Suppliers that learn a company's secrets may move into their markets. However, they would have to overcome the entry barriers placed by the brand-identity and experience that the original company has, and may need to move away from their own core competences so as to develop new ones in order to compete effectively.
- If multiple sub-contractors are not available then dependence is a problem. However, if routes to multiple sources and additional sub-contractors are identified then this dependency may be reduced.
- If sub-contractors are far away, then the learning that comes from day-to-day contact will be lost. However, the skills that would be learned are not key to the business, and methods of managing sub-contractors at arms-length can be developed.

So in general it is believed that the advantages of the networked organisation far outweigh the disadvantages. This certainly seems to have been the case for the companies discussed in the case-studies later in this chapter.

3.3 Why should SMEs use ASICs?

3.3.1 Use of ASICs to gain marketing advantage.

Michael Porter (Porter, 1985) defines a number of approaches to gaining sustainable competitive advantage. These are summarised in *Figure 3-3*.

		Competitive Advantage	
		Lower Cost	Differentiation
Competitive Focus	Broad Target	Cost Leadership (Nissan)	Differentiation (Ford)
	Narrow Target	Cost Focus (Lada)	Differentiation Focus (Morgan)

Figure 3-3. Porter's marketing approaches applied to the motor industry.

Porter maintains that two basic marketing approaches can be adopted in order to produce a successful product. These are either to produce a lower-cost version of an existing product and so gain market share, or to produce a product which differentiates itself from its competitors by having new or unique features. Either of these approaches can lead to a competitive advantage. The company must then decide whether to aim its product at a

wide, and consequently varied, market, or to focus on a narrow market with a product aimed specifically and closely at that narrow market and so gain a large market share.

Figure 3-3 relates these approaches to the motor industry (McArdle, 1992). Nissan, and other Far-East manufacturers gained their initial market share by producing 'copy-cat' products at a lower cost, aiming their products at a wide mid-range market. Lada or Skoda on the other hand, while adopting a low-cost approach, also addressed a much smaller and focused market at the low-price end of the vehicle market. Ford, and perhaps Rover, aims to produce a wide range of cars which should differentiate themselves with additional features, while companies like Morgan, and Rolls Royce produce highly differentiated products aimed at capturing a large share of their respective markets. Each of these companies has been successful in its approach, but those approaches are significantly different.

Some problems do arise when trying to apply the Porter model to real cases. For example, the model discusses cost leadership in the context of manufacturing at a lower cost, but does not discuss the effect of price. In many markets (including ASICs) selling price is market-driven rather than being cost-driven. The model also seems to regard cost and features as absolute entities. In many markets it is the perception of position rather than its reality that is important, and those perceptions are relative. One person's perception of high cost or price may be significantly different to that of another.

Other models suggest a more complex set of criteria for establishing competitive advantage, and suggest that different companies can adopt different mixes of these components. One such model is shown in *Figure 3-4*.

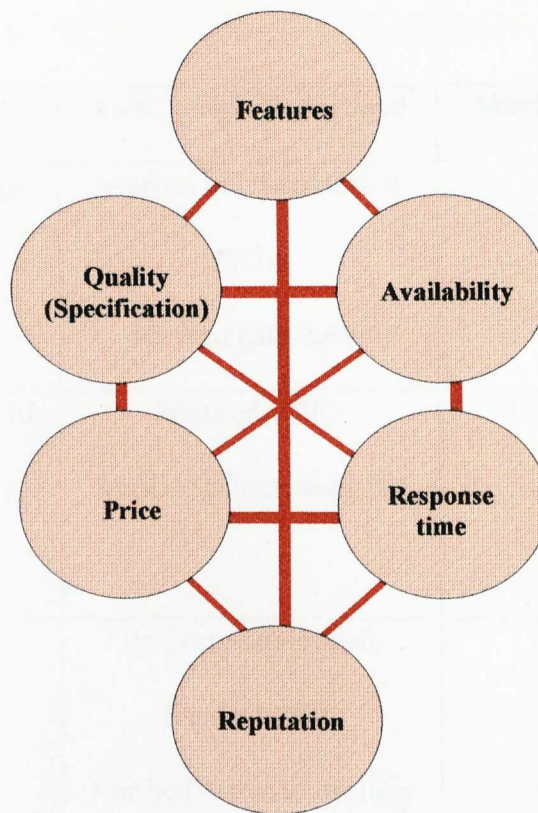


Figure 3-4 The marketing mix.

This model considers that competitive advantage is derived from a mixture of the six criteria shown in the diagram, and that these criteria are related to each other. For example, a company's reputation is obviously based on the other five characteristics. However, it must be remembered that a customer's perception of these characteristics is as important as the reality of them. It is no use having a fast response-time if nobody knows about it, or if response time is not important to a company's customers.

The use of ASIC technology has permitted different mixes of these marketing approaches to be followed by a number of successful large and small enterprises. Five examples of how SME organisations have used ASIC technologies in different ways to generate successful products are discussed in the following section. Their approaches are summarised in *Table 3-4*.

Company & Product	ASIC technologies used	Marketing approaches
Fraser-Nash Technology <i>Adhan alarm clock</i>	Masked microcontroller FPGA Masked gate- array	Availability Features Quality
TRACKER Networks Ltd. <i>Stolen vehicle tracking system</i>	Masked CBIC Masked Microcontroller	Differentiation Availability
Ionica Ltd. <i>Radio local-loop telecommunications system</i>	Programmable logic Masked ASIC Masked microcontrollers	Cost leadership Price Differentiation Features
Waterside Ltd. <i>Water softener</i>	User programmable microcontrollers	Features Differentiation Quality
HJ Weir Ltd. <i>Laundry equipment</i>	User programmable microcontrollers	Features Quality Response time

Table 3-4. Summary of case studies

3.3.2 Fraser-Nash Technology: ASICs in a domestic product.

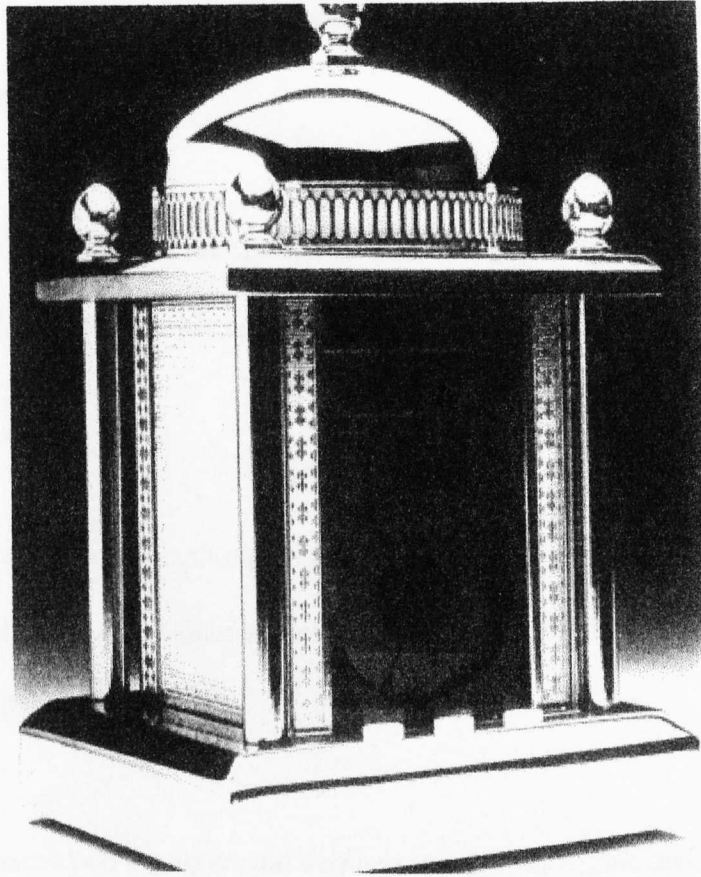


Figure 3-5. The Adhan alarm clock

Fraser-Nash Technology is a company engaged in the design and manufacture of a wide range of products destined for both high and low-volume manufacture for domestic and overseas markets. The product discussed here is the Adhan Alarm, which is a special Islamic, electronic alarm-clock. The product is intended for sale to followers of the Islamic faith. It serves to remind them of prayer times and give an indication of the direction of Mecca, the holy city. This case study is developed from the product literature for the alarm, a case study presented in a DTI seminar (Ivey, 1994), and a DTI leaflet (DTI, 1996:3). The product is shown in *Figure 3-5*.

The product has a number of unique features:

- It automatically performs the astronomical calculations necessary in order to calculate the times of prayer
- It generates an authentic Adhan ‘call to prayer’ using synthesised speech at appropriate times in addition to having sounds suitable for more usual alarm clock functions (e.g. ringing bells)
- It has a solid state electronic compass and is able to calculate and display the bearing to Mecca based on an internal database of the latitude, longitude and time zones over 1500 cities worldwide
- The product drives two liquid crystal displays using both Arabic and English fonts

The product clearly requires a high degree of computational power combined with light weight and a requirement to be battery powered. Microelectronic devices were the obvious choice of implementation technology. Indeed, it is difficult to conceive of a portable device that could be produced without the use of microelectronics.

Price was also considered important so as to appeal to as large a market as possible, and ‘time to market’ was seen as critical as rumors of a number of competing products were emerging as the design progressed.

It was always envisaged that the product would use ASIC devices, and three different types of ASIC device were used. The devices and the way in which the functions are split between them are shown in *Table 3-5*. This table also introduces the design approach adopted by Fraser-Nash Technology and their suppliers.

ASIC Technology	Application
Microcontroller	Overall control, Astronomical calculations
FPGA	Prototyping of sound and character generation
Gate Array	Low-cost production part equivalent to FPGA

Table 3-5. Technologies used in Adhan alarm

The designers decided that the risks inherent in going straight to a masked ASIC device were too great, as the product contained a number of unproven functions such as those associated with the voice compression and decompression functions, and the driving of the graphical displays using Arabic characters. Consequently, these functions were prototyped using FPGA technology. The designers used an Altera MAX device to make a prototype of these functions and later had the design converted to a gate-array using a semi-automated process. This approach is available through a number of suppliers, and is discussed more fully in *Chapter 7*. These suppliers take a net-list of the FPGA design, convert it into a net-list for the masked ASIC family, and produce masked ASIC devices (in this case gate-arrays) based on the FPGA design. The device is simulated before and after conversion so as to ensure that the functionality is conserved in the conversion process.

This design flow is often adopted in complex masked ASIC designs or those in which some function of the circuit is untried. However, this approach needs careful consideration compared with alternative approaches such as using simulation to prove the design prior to production of a masked device. Simulation can often test the new function far more fully' and over a greater spread of production tolerances, than can be achieved by prototyping using programmable devices.

The design-flow used for the ASICs produced for this product is shown in *Figure 3-6*.

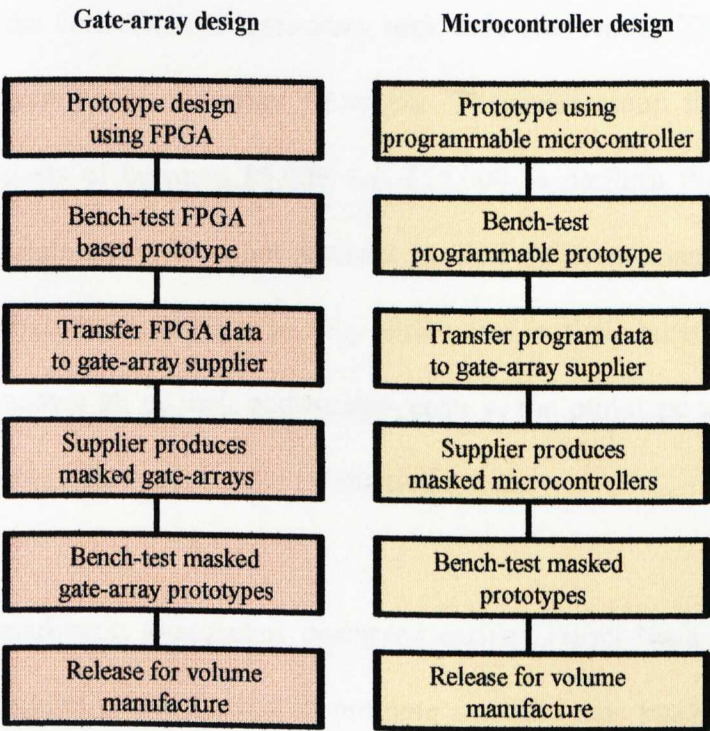


Figure 3-6 *Parallel design flows for gate-array and microcontroller*

The development route for the microcontroller is very similar to that of the gate-array in that it is possible to use programmable parts as a precursor to committing to the costs and production timescales inherent in producing a low-cost masked part. This is more normal

in microcontroller design as the complexity of the software design often precludes the use of simulation to prove the design.

The gate-array development produced a 'right-first-time' part which was ordered in high volume at the prototype stage in order to meet tight development time constraints. This enabled the company to quickly come to market with a product that has gained widespread acceptance and has sold in large volumes.

The company state that the complete design up to prototype using FPGAs took four months, and that the conversion to gate-array took only two weeks. The first production volumes (20,000 parts) took a further 12 weeks. They also claim that different ASIC suppliers quoted costs of between £6,000 and £25,000 to perform the translation from FPGA to masked gate-array. It is not unusual to find different manufacturers quoting widely differing engineering charges as they differ also in their business models. Some suppliers aim to recover all of their engineering costs at the prototype stage, while others are prepared to recover the costs in later production orders.

In terms of the marketing approaches discussed earlier, Fraser-Nash Technology were using features, availability and quality to promote a totally new product that would not have been possible without the use of microelectronics. Price is also important in a high-volume domestic product of this type.

Fraser-Nash Technology can also be considered to be a networked organisation as although they performed the initial design of the FPGA and microcontroller software themselves, they used external specialist designers to perform the conversion to masked gate-array.

This approach enabled them to achieve a fast 'time-to-market' and launch a successful product.

However, it is important to realise that single product successes do not necessarily ensure long term business success. At the time of writing reports are starting to appear alleging that Fraser-Nash Technology is experiencing business difficulties (BBC Radio 4, May 14th 1997). In spite of this, the product remains an excellent example of how ASIC devices can be used by a small company to bring a new and innovative product to market in a relatively short time.

3.3.3 TRACKER Networks®: Mixed signal ASICs and masked microcontrollers in a stolen vehicle tracking system.

Each year over 200,000 cars are stolen in the UK. TRACKER Networks is a UK company established in 1993 to operate a radio-based stolen vehicle recovery system. Since its launch, it has been responsible for the recovery of over 1000 stolen vehicles that had been fitted with its tracking device. Police are able to track stolen vehicles using equipment located on top of the police car dash-board as shown in *Figure 3-7*.

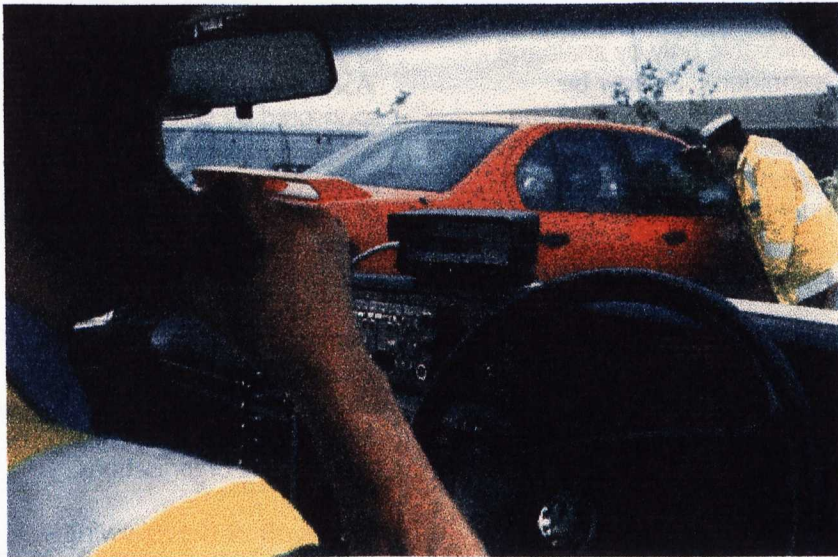


Figure 3-7. Tracker Networks stolen vehicle recovery system.

The operation of the system is shown schematically in *Figure 3-8*.

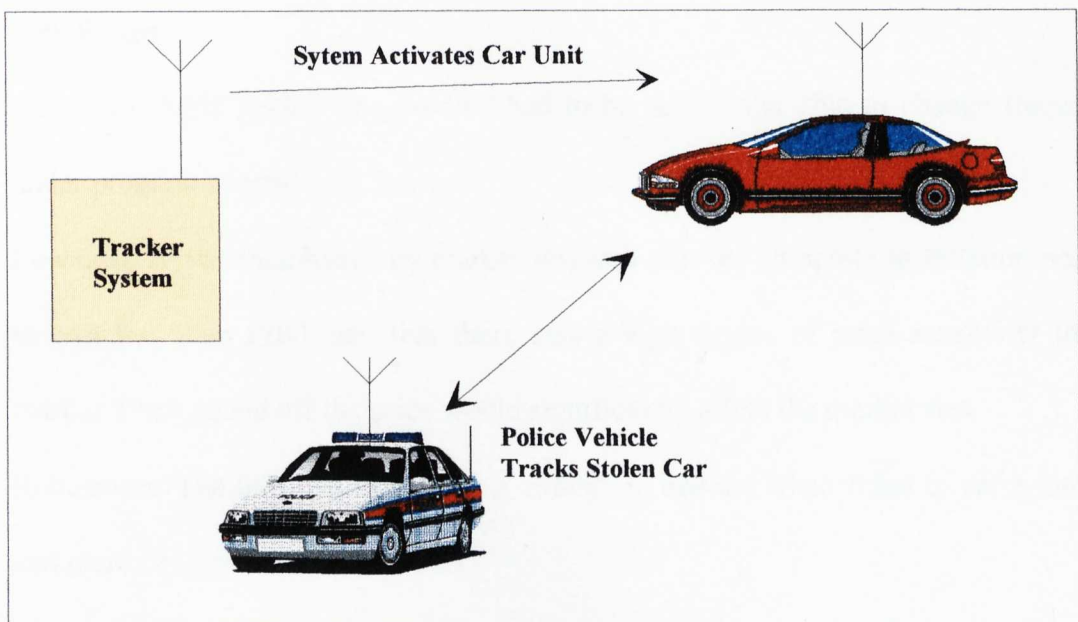


Figure 3-8. The TRACKER system.

If a vehicle is stolen, the owner contacts the network operator. The operator transmits a wake-up signal to a radio transceiver hidden in the stolen vehicle, which then transmits a homing signal which can be tracked by direction finding equipment in the police vehicle. The device in the police car (see Figure 3-7) displays the direction to the tracked vehicle, the approximate distance from the tracking vehicle, and the identity of the tracked vehicle. The system has been widely reported in the UK electronics press (McArdle, 1994. MacLeod, 1994).

The vehicle transceiver had a number of marketing and technical requirements, which included:-

- **Small Size.** The unit needs to be concealed easily in a small car.
- **Low Power Consumption.** The unit is battery powered and must continue to transmit for a long period until recovered.

- Low Weight.
- Frequency Agile Radio. The product had to be secure and able to change frequency under program control.
- Low cost. It was established by market research that the complete installation needed to cost less than £200, and that there was a high degree of price sensitivity in the market. Each pound off the price would significantly affect the market size.
- Robustness. The unit had to be robust enough to operate when fitted to earth-moving and plant equipment as well as cars.
- Intelligence. The unit needed to overcome basic counter-measures (e.g. jamming).

This combination of requirements led to implementation shown in *Figure 3-9*.

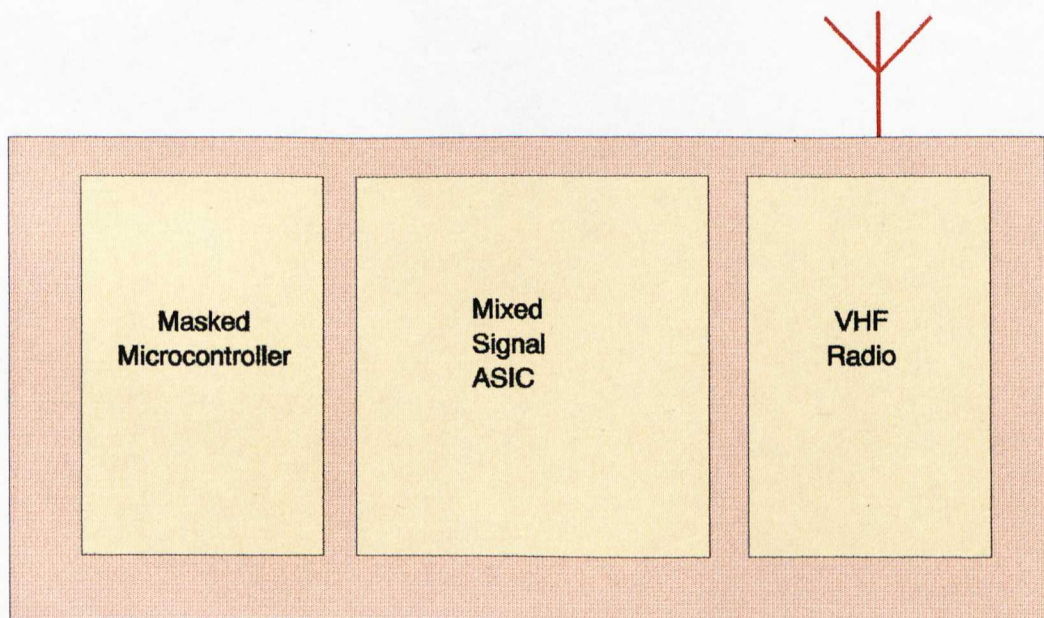


Figure 3-9. TRACKER vehicle transceiver, block diagram.

The unit used two ASIC devices. A masked microcontroller (Motorola 68HC05) was used to provide overall control and protocol handling. This also allowed the flexibility to

change some features of the product at a lower cost than those involved in making design changes to the mixed-signal ASIC, which would incur high NRE charges from the silicon vendor. This was important if a differentiated product was to be maintained at low cost.

The mixed-signal ASIC used in this design was a GEC Plessey Semiconductors 70K series standard-cell device. It was used to perform all of the well-defined processes that were unlikely to change in future developments of the product. The cost of changing such a device is high, as it involves significant re-tooling costs by the semiconductor manufacturer. This makes it unattractive to go through changes for a minor improvement in features. The mixed-signal ASIC performed the following functions:-

- Frequency Synthesis using a Phase Locked Loop and a Frequency Locked Loop which could be programmed by the microcontroller so as to change local oscillator (LO) frequency. The LO operated at around 200 MHz
- Modulation and Demodulation of the data stream. This included a fairly complex data and clock recovery system incorporating a Viterbi Decoder fabricated by designing a reduced instruction set DSP processor into the ASIC.
- Power Supply Control.
- Reference Oscillator and Crystal Compensator. The crystal used for the reference oscillator is automatically adjusted to compensate for temperature and aging, allowing a low cost crystal to be used and still maintain 2ppm accuracy in frequency.

The design, performed by Plextek Ltd., used about 13,000 gates of digital logic, which along with the analogue components gave the ASIC a total die size of less than 50 square millimeters. The mixed-signal ASIC had an NRE of a few tens of thousands of pounds and

a volume part cost of a few pounds (exact figures are not given here for reasons of confidentiality).

The final result was a successful product which sells in large quantities (tens of thousands per annum), and has become a factory-fitted option on the vehicles produced by a number of manufacturers. In its first year of operation the system was responsible for the recovery of over 250 stolen vehicles, and by early 1996 the system had recovered over 1000 stolen vehicles. Tracker Networks have succeeded in bringing an innovative product to the market which is only made financially viable through the use of advanced mixed-signal ASIC and microcontroller technology.

In terms of the Porter model discussed earlier, this product is clearly differentiated from other vehicle security products (e.g. car alarms) by its features, and is able to take a cost and price-leadership position in relation to other vehicle location systems (e.g. Securicor Datatrac) in what has been shown to be a very price sensitive market. In terms of the marketing-mix model (*Figure 3-4*), TRACKER uses price, availability to the mass market, and features (such as the recent introduction of a data up-link) to give the product competitive advantage. This competitive advantage is contingent on the use of two ASIC technologies (mixed-signal ASIC and masked microcontroller).

The structure of TRACKER is that of a networked company. In addition to out-sourcing research and development, the company also sub-contracts the manufacturing of the product to a number of overseas companies. Installation of the equipment in vehicles is also sub-contracted to trained installation companies.

3.3.4 Ionica Ltd: Domestic telephony using radio

The final connection between a telephone exchange and a subscriber's telephone is known as 'the local loop'. Traditionally, this link has been provided almost exclusively by British Telecom, mainly due to the high cost involved in road works to install cables. In 1992, Nigel Playford had the idea of using radio to make this final connection, and formed Ionica Ltd. to exploit the idea. The system, and its relation to the standard switched-network is shown in *Figure 3-10*. Ionica is able to operate a local infrastructure using its own equipment, and communicate with the greater telephone system at the trunk level (generally at data rates of 2Mbits per second and greater). This trunk capacity can be purchased from a number of suppliers (e.g. BT, Mercury, Energis and others)

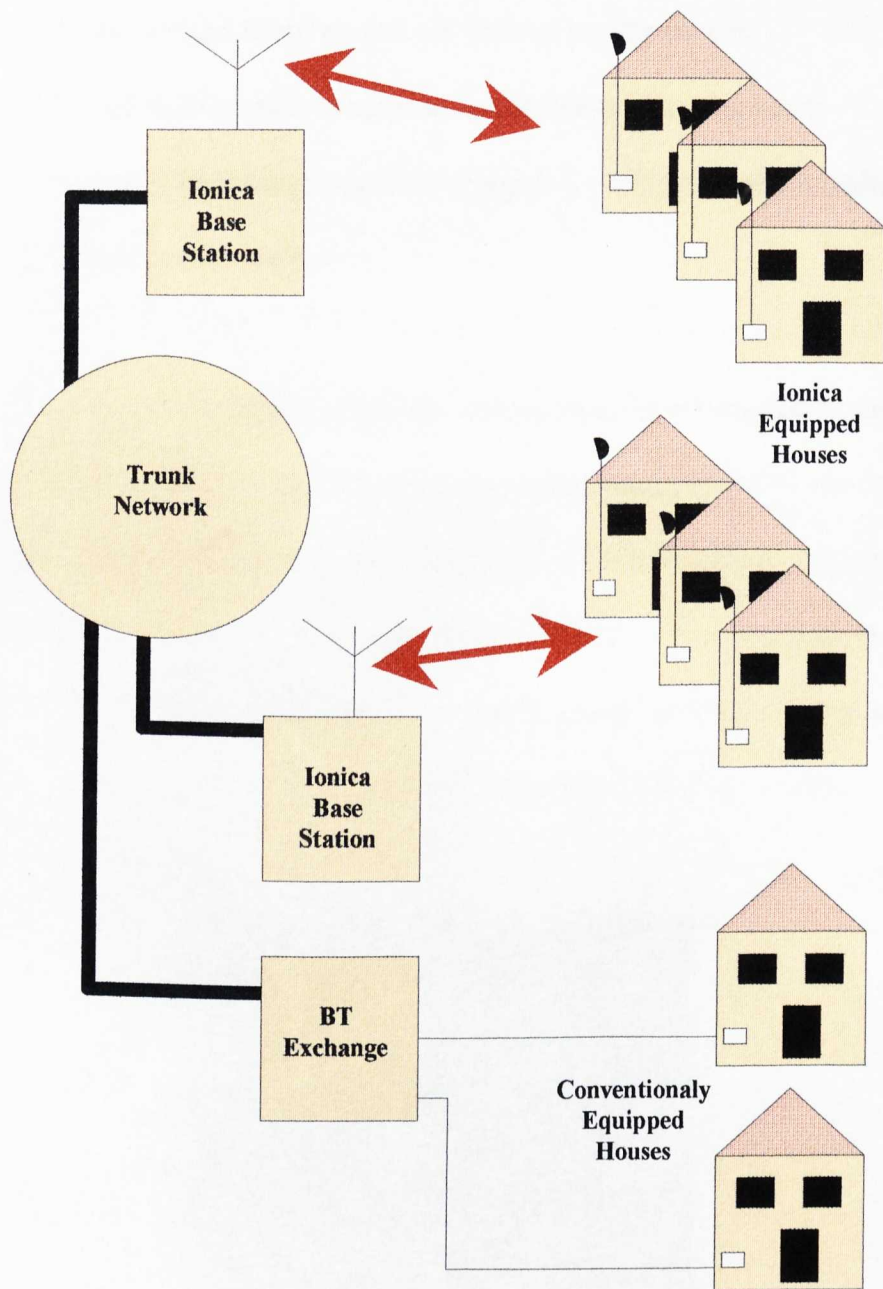


Figure 3-10 The Ionica system.

Right from its beginning in 1992, Ionica made a policy of not creating internal research and development groups, but instead forming close relationships with a number of design consultancies or ‘development partners’ some of whom became early shareholders in the company. This approach gave Ionica a number of distinct advantages including:

- Immediate access to established design teams

- The ability to turn design teams on and off without significant cost
- Access to a broad skill-set able to adapt to its constantly changing needs
- Access to advanced technology suppliers through the links that the established design consultancies had already built.

As a result of these relationships, Ionica was able to grow at a remarkable rate (over 150 staff by 1995) and raise large sums of investment capital (over £100M by the end of 1995). The company was also able to develop equipment at an accelerated rate. For example, initial demonstrator equipment of the type shown in *Figure 3-11* (which includes FPGAs, microcontrollers and PLDs in addition to sophisticated radio frequency components operating at 3.5 GHz) was developed and produced in less than seven weeks.

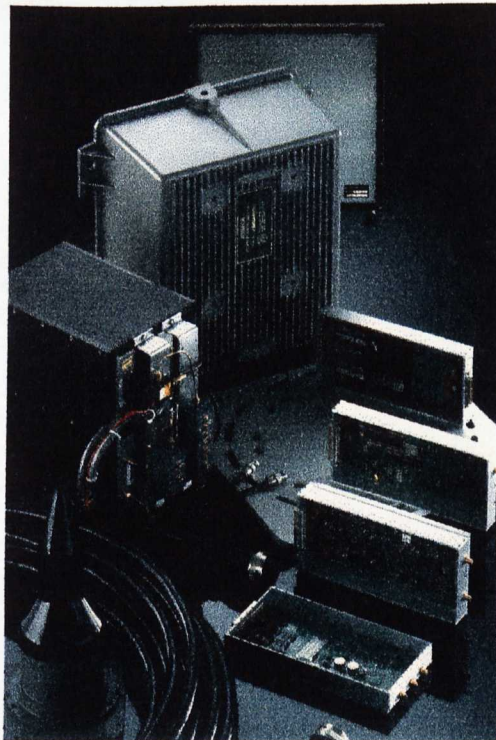


Figure 3-11. Ionica Link Equipment

The entire system was developed in time for a launch in May 1996 (the final system also made extensive use of all types of ASIC discussed in this study). The requirement for low manufactured cost meant that ASICs were used extensively at all stages of the product. Indeed, the whole concept would not have been feasible without the use of ASICs, and would not have been achieved in the tight timescales without the use of third party design skills in Ionica's 'development partners'.

In terms of its structure, Ionica is a classic example of a networked company. All of the research and development for the system was out-sourced, and all of the equipment used in its products is manufactured by sub-contract manufacturers. These manufacturers have also been licensed to market the equipment in other countries.

In terms of the marketing models, Ionica has been able to use cost-leadership to launch a UK product with call charges 15% less than those of BT. The system also has some features that are not available from its competitors, such as a two-line system for no extra cost. This is because the technology is designed to multiplex multiple calls over a single radio channel, so the additional 'line' comes with little extra cost to the supplier.

In relation to the Porter model (*Figure 3-3*) they have used both differentiation through additional features and cost leadership across a broad target (the domestic telephony market). This somewhat contradicts the Porter model which suggests that cost-leadership and differentiation are to some extent mutually exclusive. This contradiction can be seen in other case-studies discussed in this chapter. However, the marketing mix model (*Figure 3-4*) better describes Ionica's approach. They have used a mixture of price and features to

give them a marketing advantage over their major competitors. Their competitors on the other hand have reputation and availability working in their favour, at least until the Ionica system becomes available nationwide over the next few years, and its brand identity becomes stronger than it is at present.

3.3.5 Waterside Ltd: Adding intelligence with a microcontroller.

Waterside Ltd. develop water softeners for the domestic and export markets. In 1995 they decided to develop a new, innovative valve mechanism with fewer moving parts than their competitors' products, and using advanced plastic molding techniques to reduce costs. Water softeners function by the process of ion-exchange. Water is passed through a resin chamber where 'hard' calcium and magnesium ions are exchanged for 'softer' sodium ions. However, the chamber must be periodically 'regenerated' by flushing with brine. It is the control and efficiency of this regeneration process that governs the cost, size, and competitive position of water softeners (Mace, 1996). The valve assembly and electronic controller of the new range of softeners is shown in *Figure 3-12*.

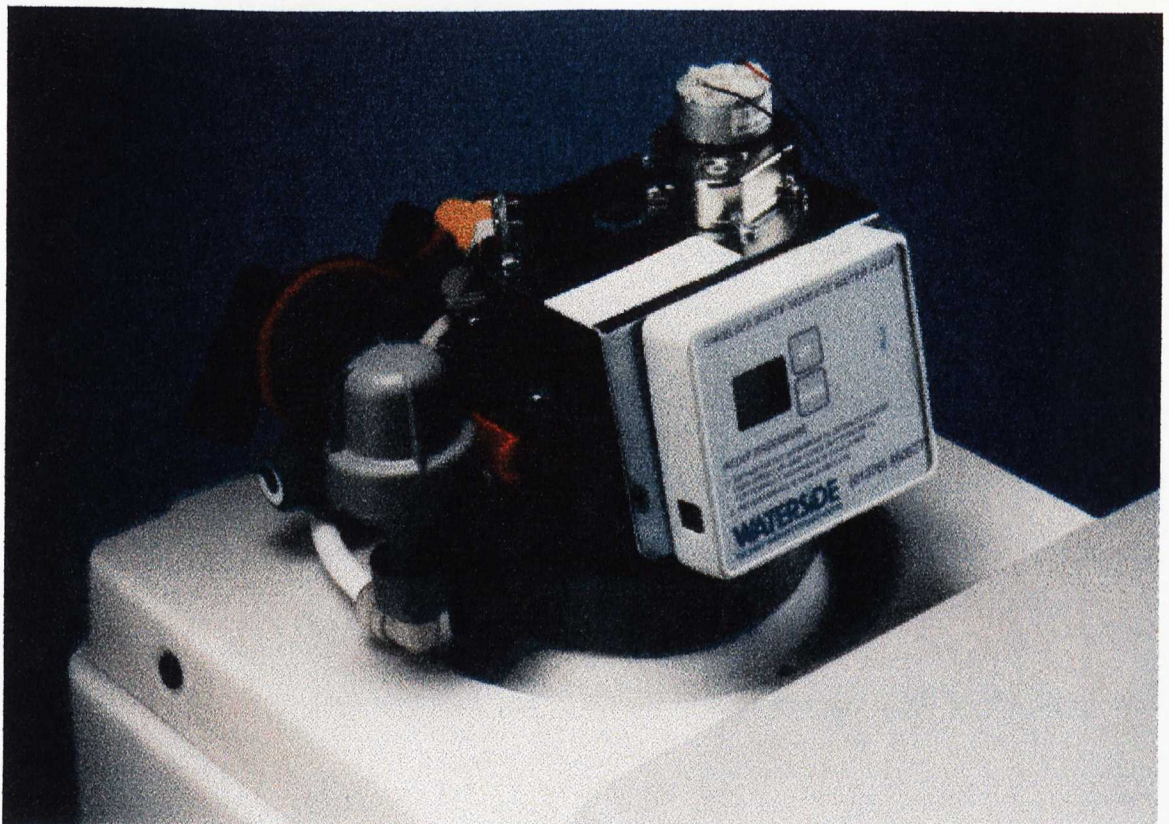


Figure 3-12. The Waterside water softener

Traditionally, water softeners had electro-mechanical controllers, similar to elementary central heating controllers, but these had a number of disadvantages including:

- They needed to be reset after power-failures and on changes to/from summer time
- They initiated a regeneration at a set time interval irrespective of water usage

The new electronic controller overcomes these problems by using a microcontroller to bring intelligence to the control mechanism. It is able to add the following features.

- Water usage is measured using a flow sensor in the output stream of the valve, and the pattern of water usage for a particular household determined over an extended period. This pattern is then used to predict the most likely optimum regeneration time. (i.e. at a time of low water-usage before the ion-exchange chamber is exhausted)
- The need for a clock is removed, as absolute time of day is irrelevant to the regeneration algorithm. The algorithm is based on a rolling two week period relative to the current time. It calculates the best regeneration point relative to the current time, but has no need to know what time of day this corresponds to.
- Optimum regeneration reduces the amount of salt that the unit uses, and consequently allows the unit to be built with a smaller resin chamber and salt vessel. This results in a smaller overall size and lower cost.
- A simple, intuitive user-interface via a liquid crystal display and a few keys was implemented.

These new features allow the product to be differentiated from its competitors. Additionally, the knock-on effects of using the microcontroller simplified the non-

electronic parts of the product so that a smaller, lower-cost unit could to be launched at a low price. This was made possible by the intelligence that a simple microcontroller can bring to a product at very little cost. This case is also in slight contradiction to the Porter model which suggests that cost-leadership and differentiation should be mutually exclusive. In terms of the marketing mix model (*Figure 3-4*) the company uses a mix of low price, additional features, and the company reputation as a brand leader to give them competitive advantage.

Waterside is another example of a networked company. Although they perform final assembly of the product, most of the major components are designed and manufactured on a sub-contract basis.

3.3.6 HJ Weir. Microcontrollers in bespoke laundry machines

HJ Weir Ltd. was established in the 1950s and has grown to a company with an annual turnover of £3.5M. It manufactures industrial laundry handling machines which are used in laundries in hospitals, hotels and other large linen users throughout the world. The machines are able to line up linen for ironing machines, fold, pack in plastic bags, and stack linen of all sizes from napkins to sheets. Each laundry installation is different, incorporating a different mix of machines, so all of Weirs systems are effectively bespoke one-off projects. A typical installation is shown in *Figure 3-13*

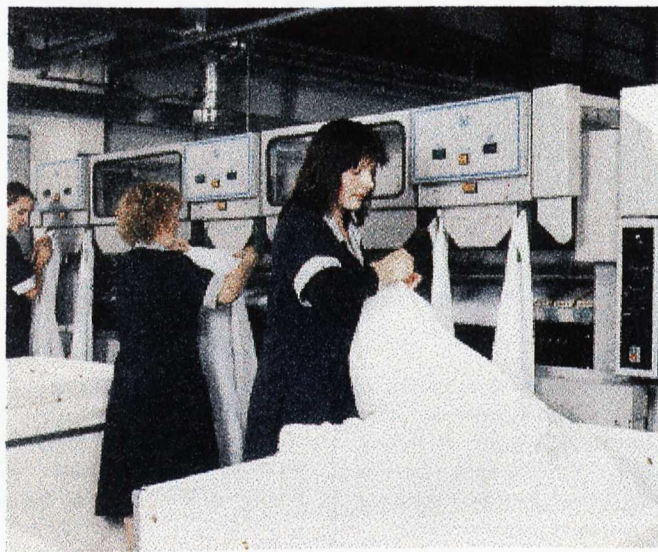


Figure 3-13. HJ Weir's Laundry equipment

Control of the machines requires precise speed and positioning control of the linen handling equipment. Back in the 1960s, this was achieved using electromechanical techniques such as switches, relays, and simple electro-mechanical timers. These techniques were notoriously inaccurate, and machines seldom ran for a great length of time without requiring adjustment.

The latest Weir machines incorporate a central controller based on a Motorola microcontroller. The microcontroller senses the position of linen using external sensors and makes decisions regarding the position of up to 5 folds in two directions. It also drives a liquid crystal display and keyboard which forms the user interface. Weir had the controller module designed by external consultants, and also have the electronic module manufactured by a subcontract organisation. The 'System 4' controller is shown in *Figure 3-14*.

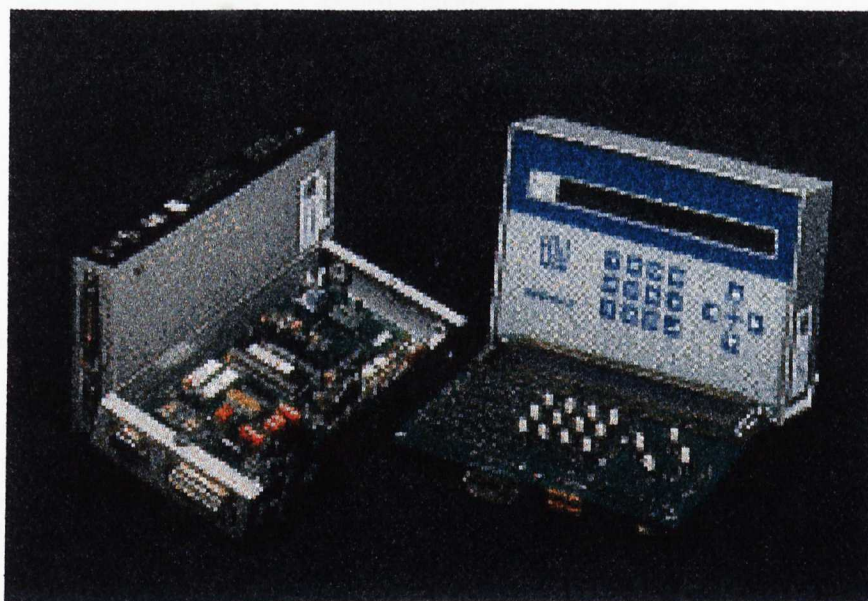


Figure 3-14. The HJ Weir System 4 controller

Weir are now fully committed to the use of microelectronics in their products and are considering a 'Fuzzy Logic' solution to future control challenges in co-operation with the Microelectronics in Business Support Centre at the University of Bournemouth. The use of microelectronics has allowed them to become a world leader, and has been cost effective even in the 'one-off' market in which they operate.

HJ Weir operate in a small, focused market. And in terms of the Porter model have been able to differentiate their products by using microelectronics to give them additional features and higher reliability than those of their competitors. In terms of the marketing mix model (*Figure 3-4*) they have used microelectronics to bring higher quality to their products through less frequent break-downs. They have also decreased their response times by being able to quickly configure new systems through the ability to program the electronic controller.

In their use of microelectronics, HJ Weir have started to become a networked company. All of the design and manufacture of the electronic sub-assemblies used in their equipment is performed by sub-contractors.

3.3.7 The case for ASICs in small businesses

The case for SMEs using ASICs to generate clear competitive advantage is shown in all of the cases in this chapter. Five small companies have developed successful products which rely heavily on the advantages that ASIC technology can bring. In each case, their business aims would have been difficult if not impossible to achieve without the use of ASICs. Fraser-Nash would have been unable to meet their cost targets, TRACKER could not have made a unit that would appeal to the mass market, Ionica could not have competed with its large multi-national competitors, Waterside could not have fully exploited the potential of their new valve technology, and HJ Weir would not have been able to easily provide flexible one-off systems in a cost-effective way.

Naturally, not every SME that adopts ASIC technology can automatically expect to produce a successful product, or to be successful in using the technology. Indeed a case study discussed in *Chapter 6* identifies some problems that a company can have in assimilating what can be a complex technology. However, the case-studies discussed in this chapter aim to show that small companies can be successful in adopting ASIC technology.

These are just five examples of how ASICs can be used to provide clear competitive advantage. If other UK companies were to adopt similar approaches, then many more innovative, successful products could be produced.

3.4 Opportunities and problems in dealing with the SME base

The structure of SME manufacturing companies has some advantages in aiding their flexibility in approach to new ideas and technology, but there are also a number of inherent problems. *Figure 3-15* summarises the results of a survey performed by the Semiconductor Businesses Association (SBA, 1996) in which design-houses were asked to compare their SME clients with their large company clients in a number of key areas.

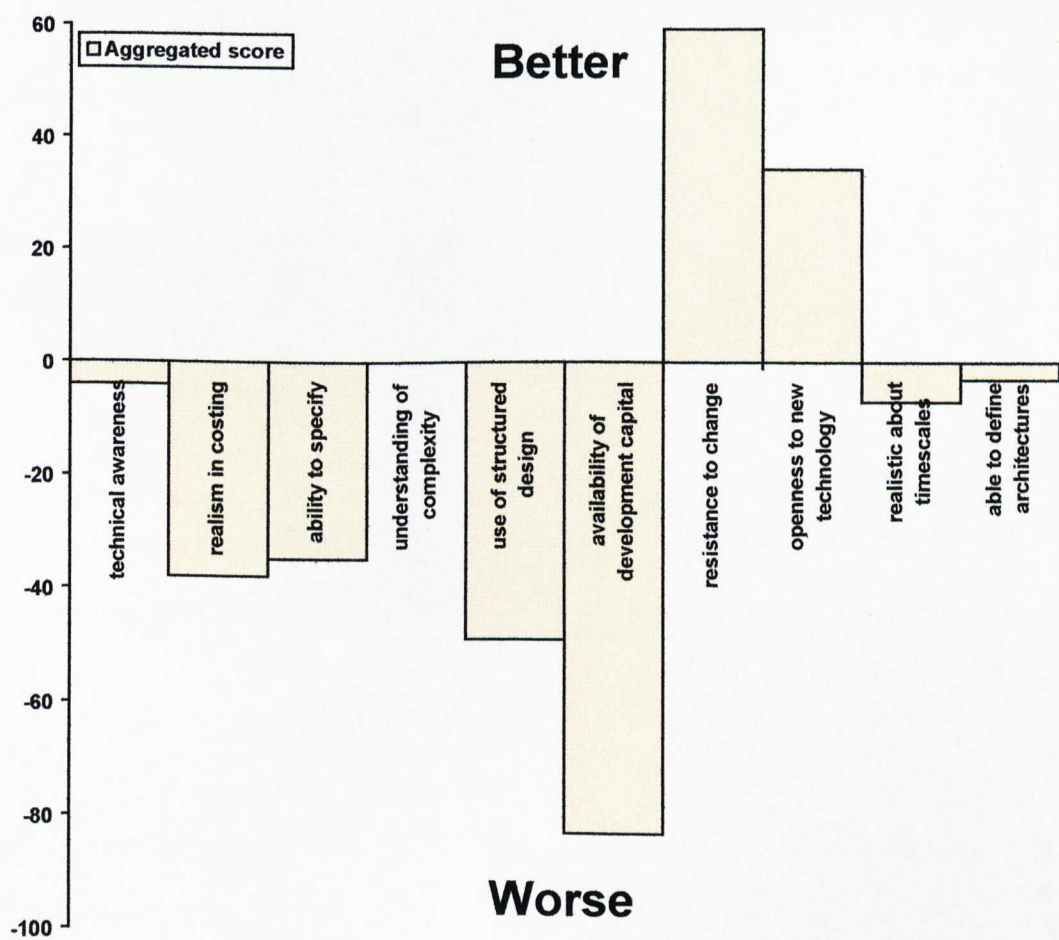


Figure 3-15. Comparison of SME and non-SME clients.

Although in many areas respondents did not see major differences between large and small companies, there were some areas in which the differences were significant. Small

companies were seen as much less resistant to change and less resistant to new technology. However, a major problem with shortage of development capital was identified in small companies, accompanied by less ability to specify or cost development programmes.

3.5 Conclusions regarding the structure of the UK manufacturing base.

The work of this chapter leads to a number of interim conclusions regarding the structure of the UK manufacturing base:

- The SME sector represents a very significant proportion of the UK manufacturing base, as indeed it does in all of Europe, and even using fairly conservative estimates, could generate in excess of 15,000 individual ASIC applications. Later chapters will show that this figure is not even remotely approached.
- The structure of small, and also large, companies in the UK and elsewhere is changing from the traditional tightly structured organisation, to a more networked structure. This has become evident in all industrial sectors and is set to continue.
- A wide range of companies operating in significantly different markets have been used to illustrate that small companies can be successful in adopting microelectronic technologies.
- The design industry perceives that SMEs can be more flexible and adaptive than their larger competitors, but that SMEs are often short of development capital, and are sometimes unrealistic in their financial appreciation of new technologies such as ASICs.

4. Previous work in the area of ASIC adoption

Literature searches and initial discussions with the supply-industry and the DTI produced a number of publications with some relation to specific parts of this research. They are referred to individually at appropriate points in this study.

Some publications of a more widely applicable nature were also identified, and these are reviewed in this chapter.

4.1 The 1991 MSA/DTI survey and report.

The most comprehensive analysis previously performed into the reasons for non-adoption of ASIC technology in the UK was that undertaken by Michael Shortland Associates (MSA) on behalf of the DTI in 1991 (Shortland, 1991). This followed a similar survey performed by MSA in 1986 which is reviewed in the same publication. The survey was addressed to potential users of ASICs within the electronics industry and considers the use of programmable logic, gate-array and standard-cell devices. It did not address the use of microcontrollers.

The main reason for the survey was to establish whether government intervention might be useful in increasing the adoption of ASIC technology, and the results of this survey were instrumental in the decision by DTI to launch the 'Microelectronics in Business' programme which will be discussed in more detail later. The main findings of the research were as follows.

In the period from 1986 to 1991, the use of all types of ASIC technology by SMEs in the electronics sector had grown from 32% of questionnaire respondents to 58%. The report assumed a total electronic SME base of around 5000 companies, implying that around 2900 UK SME electronics companies were ASIC users.

When gate-array users were considered in isolation, the report suggested that 24% of electronic SMEs were users, which would give 1219 SME users. This is somewhat at odds with the current view of the supply industry (see *Chapter 5*) which is that only around 150-200 masked ASIC designs of any kind are started each year by UK companies of any size, and only a small proportion by SMEs. In addition, respondent figures suggested that over

400 companies used cell-based devices and over 400 had custom parts. The differences between these responses and the present view of the supply industry should clearly be investigated.

Later in the report, Shortland discusses a follow-up to claims of extensive use of analogue and mixed-signal devices. The authors of the report found the reported level of use much higher than expected and so investigated it further. Further investigation showed that respondents had misinterpreted the questions and had classed their use of commodity and Application Specific Standard Parts (ASSPs) as being mixed-signal ASICs. Incorrect answering of technical questions by poorly informed users is to be expected in a survey of this kind, and is largely unavoidable. Some degree of misinterpretation may also have taken place in the other areas, due largely to a lack of understanding of ASIC technology by the respondents. However this view cannot be substantiated five years after the Shortland survey.

According to Shortland, who quotes Dataquest figures, the total UK market had grown from \$180M in 1986 to \$300M in 1991; considerably less than had been predicted in 1986. The UK had also slipped from first in the European league table of ASIC consumption to third place, behind Germany and France. In the MSA 1991 survey, the benefits of using ASIC devices were seen as (in order of importance):-

- Lower manufacturing costs.
- Smaller size.
- Lower materials cost.
- Higher performance.

In the same survey, the barriers to entry to ASIC use were seen as (in order of importance):-

- Entry cost
- Insufficient volumes
- No suitable devices
- No second source

In the case of both benefits and barriers, little had changed in the ranking of these factors between 1986 and 1991.

The questioning of the ASIC supply industry showed that they saw the major obstacles in selling ASIC to SMEs as (in order of importance):-

- Prices too high.
- Lack of knowledge about ASIC.
- Identification of prospects.

The report also concluded that although most ASIC suppliers expressed an interest in working with SMEs, few marketed directly to them, and most claimed that SME customers only accounted for a small proportion of their business. This also appears to contradict the user responses, where many SME respondents were claiming to be ASIC users, and so deserves further investigation in this study.

4.2 The 1985 Policy Studies Institute (PSI) survey.

This survey, although now over 10 years old, compares the use of microelectronics in industry in the UK, France and Germany (Northcott, 1985). Although the report is largely concerned with the use of microelectronics in the production process, for example in Computer Numerically Controlled (CNC) machines, some figures about the use of microelectronics in products are given.

The PSI study stated that the position in the three countries in relation to microelectronics was basically similar. The UK was claimed to be strongest in the use of semi-custom chips, but marginally behind Germany in overall use of microelectronics in products. The report is unclear about the distinction between these definitions. *Figure 4-1* shows the percentages of companies using some form of microelectronics in their products as reported in the PSI survey.

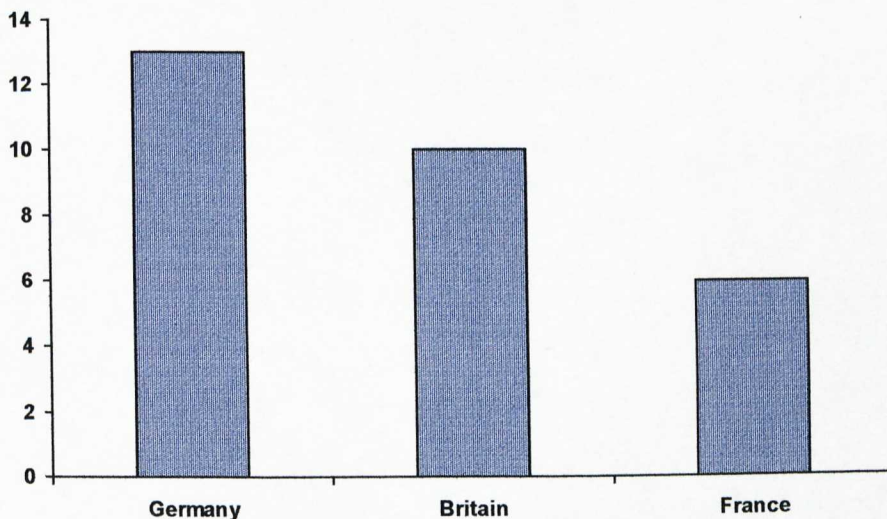


Figure 4-1 Percentage of companies using microelectronics in products in 1985

The report explored reasons for non-adoption of microelectronic technology and although the relative position changes from country to country, the main reasons are:-

- Lack of expertise
- Economic situation
- Development costs
- Development finance

These represent a slightly different set of reasons for non-adoption than those identified in later investigations.

4.3 The 1988 NEDC Report.

In 1988, the Innovation Working Party of the National Economic Development Council (NEDC) produced a report on technology transfer mechanisms in the UK & leading competitor nations. While not solely addressing electronic technology, it does contain a great deal of useful information concerning technology transfer schemes operating at that time both in the UK and overseas (NEDC, 1988).

The report concluded that the amount and level of technology transfer between academic and industrial organisations was growing in all of the developed countries considered (UK, USA, Japan, France, and West Germany). It was also noted that collaboration between industrial organisations was increasing, particularly in high risk/high investment industries such as semiconductor manufacture. It identified a number of problems within UK firms which prevented them from taking up technology which was external to them including:

- Inability to view technology strategically
- Inability to view technology as a long-term asset
- Inability to view technology transfer and accumulation as a long-term process.

The study attributes an additional set of problems specifically to SMEs including:

- Lack of time & resources to identify external sources
- Lack of suitably qualified technical specialists to be able to identify suitable technologies

The report notes that, following a 1988 government white paper on industrial policy, the emphasis of government support was shifting toward supporting small companies, and small high-technology companies in particular. This support was being provided by directly sponsoring collaborative research projects, and was moving from non-competitive to pre-competitive projects (i.e. it was moving nearer to the finally marketed product). The report also noted the increase in industrially based projects being performed by Higher Education Institutions (HEIs). This was being reflected in the growth of science parks, innovation centres and university companies.

The report also concluded that all of these trends were evident, to a greater or lesser extent in the other countries reviewed. Each of the countries was emphasising the role of the SME and promoting technology transfer from HEIs. The report does however conclude that the amount of direct financial support from local and national government is higher in USA, Japan, France and Germany than in the UK.

4.4 Lessons from the Alvey Programme.

The UK government's Alvey Programme was launched in 1983 and had a budget of £350M over a five year period to promote the development of advanced semiconductor technologies by UK semiconductor companies. The success of the programme in relation to ASIC technology is reviewed by Michael Hobday of the Science Policy Research Unit of the University of Sussex (Hobday, 1990).

Hobday accepts that as only a small proportion of the Alvey budget was aimed at improving industrial performance, the programme cannot be considered to be an industrial strategy. He suggests that having decided on ASIC as a driving technology for the programme, more emphasis should have been placed on design capability.

Hobday also states that the exploitation of ASIC by small firms will require intervention to overcome 'information failure' in the market, and suggests that future programmes should emphasise 'applications technology' rather than fabrication. He further states that support for the ASIC design sector could be important in improving the rate of ASIC adoption, particularly in smaller companies.

A more specific review of the effects of the Alvey Programme on the UK microelectronics industry is made in *Chapter 9*.

4.5 Conclusions from previously published work

The conclusions that can be drawn from the publications discussed above with respect to this study are limited, but do go some way toward proving the original hypothesis. Indications are that the UK has indeed been slow in adopting advanced microelectronic technology. The level of adoption is however unclear, and worthy of further research.

With the exception of the Shortland survey (Shortland, 1991) most researchers had concentrated on the development of the supply industry. Indeed, even national and international government funding initiatives had originally focused on the development and provision of basic technologies. To this end they had directly supported the larger companies who were able to provide such products. During the Alvey programme it became apparent that support for end-users might be a more effective use of resources, and a shift to this approach is evident in more recent programmes (e.g. Microelectronics in Business and Europractice, which are reviewed in *Chapter 9*)

The information available on reasons for non-adoption that can be derived from the publications suggests that a set of reasons was evident as early as the mid 80s. These reasons included:

- Perceived cost of entry
- Perceived lack of volume
- Perceived lack of suitable devices
- Lack of knowledge of available technologies and design methods
- Lack of marketing by suppliers to small companies
- Lack of development finance

It seemed that these reasons had changed little over a protracted period and it will be shown that they are still prevalent in the 90s.

5. The ASIC Market.

Following analysis of the report by DTI/MSA (Shortland, 1991) and initial discussions with ASIC suppliers, it became clear that the nature of the ASIC market in the UK was not clearly understood. There seemed to be large disparities in the perceived size of the market, and some false perceptions of its nature. It was considered important that the size and nature of this market should be identified before meaningful conclusions about technology adoption could be drawn.

Market information in this area is relatively difficult to obtain. Some market research organisations (e.g. Dataquest, IMS, ICE) do publish reports, but these are expensive (often over £1000 per report) and they often conflict in their findings. Consequently, it has been necessary to obtain published information from a number of primary and secondary sources including trade-press articles, marketing reports, word of mouth and a survey specifically performed for this research. It has also been possible to speak informally to researchers from the organisations discussed above in the course of the research, and obtain some of the more expensive reports through inter-library loans.

5.1 A systems view of the UK market.

In order to understand the complex, overlapping groups involved in this market and the relationships between them it is useful to use a systems approach (Open University, 1990).

One possible systems map is shown in *Figure 5-1*.

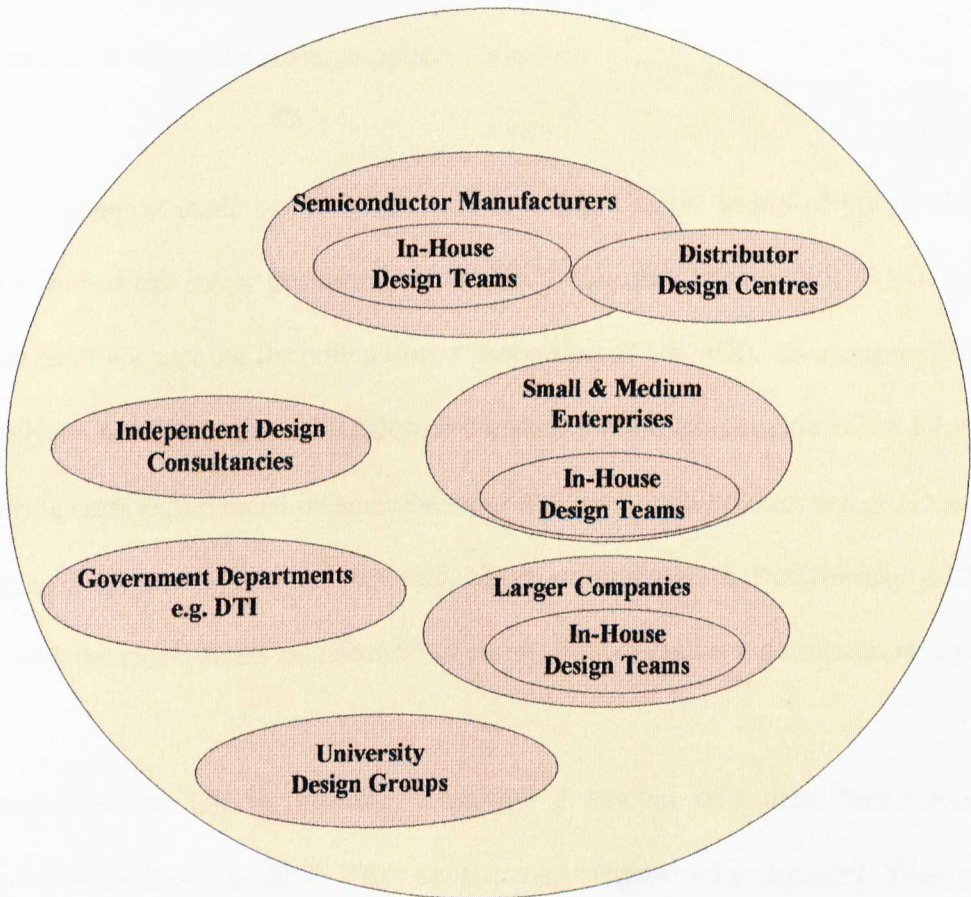


Figure 5-1 A systems map of the UK ASIC market.

The semiconductor manufacturers play an important role in the market, as they eventually supply all of the ASIC devices to final users, wherever those devices are designed.

The user base splits into two distinct groups. By far the greatest use of the technology is made by large multinational companies producing sophisticated electronic products. For

example, GEC Plessey Semiconductors claim (off the record) that 75% of their total ASIC business is done with just two customers. This group of companies would generally comprise of the large telecommunications, aerospace or computer companies such as GEC Plessey Telecommunications and British Aerospace, and would be expected to perform most of the ASIC design themselves using in-house design teams. These users are relatively few in number, can be easily targeted with a small sales force, and form the bulk of the market in which the major suppliers compete.

The other group is made up of SMEs, and is a much larger group of companies which accounts for a much larger proportion of the UK's manufacturing output. It will be shown however that they account for only a minor proportion of UK ASIC consumption. They are less likely to have in-house ASIC design capability although they do often have design engineering staff experienced in other forms of electronic and product design. Due to their number, and disparate types of business, these companies are traditionally difficult to service with the small direct salesforce that many semiconductor manufacturers have.

ASIC design in the UK is undertaken through a number of routes. Some companies (mainly the large ones e.g. GPT, BAe) have internal teams and equipment. Their product volumes are generally high, and so they tend to deal directly with the semiconductor manufacturers for all of their semiconductor requirements (not just ASICs). Some semiconductor companies have their own internal teams who are able to perform turn-key designs for customers, although this is becoming increasingly rare (e.g. LSI Logic). Some semiconductor distributors have set up design centres focused on the companies that they represent (e.g. Macro for Texas Instruments). The picture is completed by a number of independent design consultancies (e.g. Plextek, Phoenix VLSI) who are able to perform

turn-key design on behalf of clients and perform the necessary interface to the semiconductor manufacturer. This route is increasingly being taken by companies of all sizes in the UK.

Also important in the market, particularly when considering the SME, is the government. The DTI have long been involved in the promotion of ASIC technology, and the 'Microelectronics in Business' programme is reviewed in some detail in *Chapter 9*. Increasingly, government intervention in technology is becoming international in nature, with bodies such as the European Union (EU) providing grant support to research and development through initiatives such as ESPRIT. This international approach is also discussed in *Chapter 9*. The methodology of the government funded schemes often includes the design centres which have been established at a number of UK universities. The universities see their design groups as an important link with industry as well as a useful source of funding in times of reducing education spending. However, some sections of the independent design community see these centres as government sponsored unfair competition although in practice this is rarely the case as the academic centres generally perform only small developments with companies that would not usually come into contact with the design industry for reasons that are discussed in *Chapter 6*.

5.2 Methodology of investigation.

In order to investigate the nature of the market in detail, it was necessary to use a number of market research methods. Kinnear & Taylor (1987) discuss a number of such techniques classified by structure and directness that may be used for investigations of this type (Figure 5-2).

	Structured	Unstructured
Direct	Survey Questionnaire	Focus Group Interview Depth Interview
Indirect	Performance of Objective Task Technique	Thematic Appreciation Test Role Playing Word Association Sentence completion

Figure 5-2. Methods of gathering market information

For the purposes of this study it was decided to use direct methods rather than the more esoteric indirect methods as the direct methods would be likely to produce more easily interpreted results. This approach was adopted in all of the market based research performed for this study.

A number of methods were used to investigate the UK ASIC market including:-

- A questionnaire sent to suppliers of ASICs
- A review of available literature
- A constant review of the electronics press
- Analysis of reported accounts for ASIC supply companies held at Companies House
- Formal and informal interviews with ASIC suppliers and market researchers
- A review of requests for quotations encountered by the authors own company (a design consultancy which designs ASICs)
- Discussions with trade associations
- Review of commercially available market information

By using a diverse range of methods it was often possible to support the findings from one source with those derived from a completely different one.

5.2.1 The supplier questionnaire

One of the methods listed above is survey by questionnaire. It was decided that a survey of ASIC suppliers would form a useful source of information regarding market size and suppliers perceptions of the market. The design of the questionnaire is described below. The same basic approach in questionnaire design was adopted in the preparation of the other questionnaires designed during this research (i.e. The User Questionnaire, The University Questionnaire, The Embassy Questionnaire).

Participant identification.

It was decided that, given the limited number of ASIC suppliers active in the UK market, a census rather than a survey would be used (i.e. all suppliers rather than a statistical sample

would be approached). It was therefore necessary to identify one or more named individuals in every supply company known to be operating in the industry and send them a copy of the questionnaire and a letter explaining the purpose of the research. In most cases these individuals were Marketing Directors of the company concerned. They were identified from two main sources:-

- personal contacts of the author
- named contacts in the DTI's 'Custom Circuit Handbook'

Consequently, fifty questionnaires were dispatched in June 1994 to people employed by 29 different semiconductor manufacturing companies. Those companies not replying within 2 weeks were reminded by fax. This caused a further flow of responses. Within 4 weeks of the survey being sent out, 16 companies had replied, leaving 13 outstanding. Further individual letters were sent to those companies during September and October 1994, and personal visits were made to their trade stands at the UK Silicon Design Show in October 1994 and Electronica in Munich in November 1994, which caused 2 further replies. In total 18 companies replied leaving 11 for which market-share figures had to be extrapolated from other sources such as those discussed above (e.g. annual reports and informal interviews).

Questionnaire design.

Questionnaires are generally considered to have five main sections:-

- Identification Data. The title of the questionnaire.

- **Classification Data.** Concerning the characteristics of the respondent.
- **Request for co-operation.** Designed to enlist the respondents help.
- **Instructions.** Comments to the respondent on how to use the questionnaire.
- **Information Sought.** The body of the questionnaire aimed at gathering the required information.

Identification data.

The questionnaire was identified as, 'Questionnaire on the UK ASIC market & the use of ASIC technology by small & medium enterprises in the UK'

Classification data.

Classification data is made up of contact details for the respondent, and question 1 which ascertains the types of ASIC that the company supplies.

Request for co-operation.

The request for co-operation was made in the letter accompanying the questionnaire. In addition to explaining the purposes of the research, the respondent has further encouraged to return the questionnaire by:-

- Including a return envelope with a real stamp (in the author's experience in other surveys people have been shown to be more likely to return these than 'business reply' envelopes).
- Promising a donation to a children's charity for every returned questionnaire. A donation was made to NSPCC in consequence.

Instructions were given with each question, and the questionnaire ends with thanks for the respondents co-operation and instructions for its return.

Information sought.

The questionnaire (see *Appendix A*) was intended to ascertain information in a number of areas including:-

- Identification of which companies were active in each of the technology areas
- Identification of the market share that each company had
- The perception of total market size held by each company
- Actions taken by each company to promote the use of ASICs by SMEs
- The perception of the respondent to SMEs in relation to ASIC technology

The first two areas were approached directly. Questions 1 and 2.1 ask the respondent to identify the technologies which they supply and the number of designs that they have taken to prototype in each of them in each of the previous five years for UK based companies. They are then asked (in 2.2) to identify the proportion of those designs that were for SMEs. SMEs are defined at this stage to prevent misunderstanding.

The next two questions, regarding total market size, elicit perceptions as well as factual replies. This approach was taken because informal discussions with ASIC suppliers revealed that few if any had a clear idea of total market size gained through real research. In most cases replies were based on rough sales forecasting or previous sales. However, the views held by people working in this area are clearly important and likely to be reasonably accurate if a consensus is achieved.

Question 3 asks the respondent to show which marketing techniques their company uses to encourage SMEs to adopt ASIC technology. Both previous and planned future initiatives are requested. The list of possible answers came from discussion with suppliers and personal experience of the author. An open 'Other' box is given so as to elicit information about unusual or unique techniques that might be being used.

Section 4 aims to elicit information in a number of ways. Firstly, each question addresses a specific problem or question often associated with the adoption of ASIC technology (e.g. ability of engineers, sales volumes, cost of entry). These statements are drawn from discussions with semiconductor suppliers, earlier research and personal experience of the author. Secondly, there is a balance of questions between positive and negative attitudes to the use of ASICs by SMEs, so that they can be used to ascertain an overall attitude of the respondent to ASIC use by SMEs without introducing bias. The answer section for these questions is in the form of a set of Likert scales with an even number of agree and disagree responses. This forces the respondent to give either a positive or negative answer rather than a non-committal midpoint answer. Analysis of numeric scores can be used to assess the degree of agreement or disagreement with the statement.

5.3 Total semiconductor market: UK, Europe & World

Estimates of the absolute size of the semiconductor markets in the UK, Europe, and the world vary slightly from survey to survey. Industry in the UK generally accepts the figures from Dataquest, FEI, and some other market research organisations. An aggregation of available data and forecasts from a number of organisations over the period of this research is shown in *Figure 5-3*.

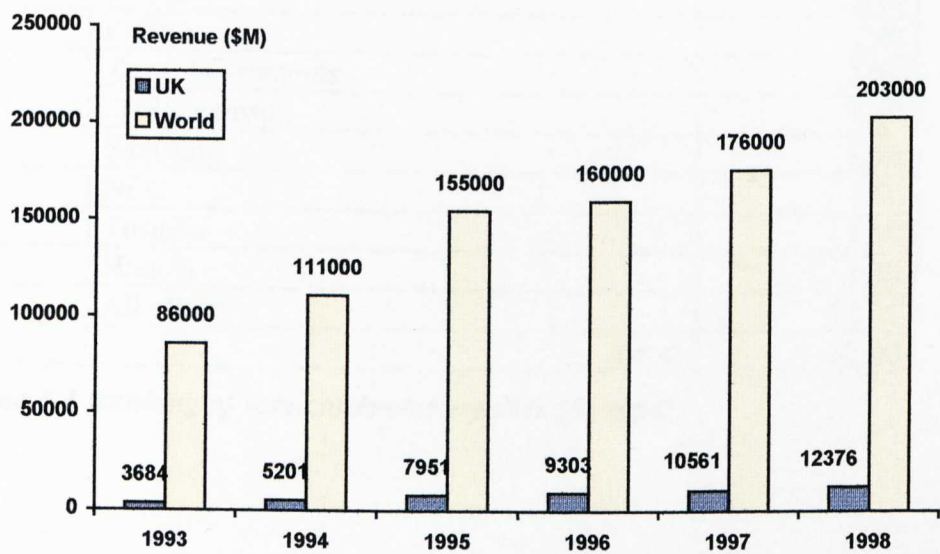


Figure 5-3. UK and world semiconductor market.

In 1995 the world semiconductor market grew by 40% to reach \$154.7bn with Europe growing by 45% to reach \$30bn. The UK market in the same year reached \$7.9bn and so accounts for 26% of the European total. This puts the UK in second place in the ranking of European consumption, slightly behind Germany. In the last few years, growth has been higher than the market pundits predicted, leading some to say that a slump is in prospect and that the slump in DRAM prices being experienced in mid 1996 is the first sign of this.

In early 1996, Electronics Times reported Dataquest figures suggesting that the ranking of semiconductor producers servicing the European market was that shown in *Table 5-1* (Walko, 1996).

1995 Rank	Company	1995 European sales (\$bn)
1	Intel	3.48
2	Motorola	2.15
3	Siemens	2.12
4	Philips	1.69
5	Texas Instruments	1.60
6	SGS-Thomson	1.59
7	Samsung	1.56
8	NEC	1.52
9	Toshiba	1.10
10	Hitachi	1.10
	All others	12.21
	Total	30.08

Table 5-1 Ranking of semiconductor vendors (Europe)

This position is not as positive for the UK as it may at first seem. Bernard Courtois of the French institution TIMA (Techniques of Informatics and Microelectronics for Computer Architecture) points out that although the UK represents about a quarter of the European semiconductor market by revenue, most of these parts are specified and ordered by non-UK companies (Courtois, 1994). The implication is that although using the technology in its factories, the UK's designers have not adopted ASIC technology to the extent that the gross consumption figures might suggest.

Indeed, 69% of UK semiconductor consumption is specified outside of the UK (41% by American companies, 16% by Japanese, and 12% by companies from continental Europe). Courtois considers that the UK electronics industry is composed largely of, 'screwdriver

factories'. (Courtois, 1994). He prefers to define the European market-split in terms of 'European deciders' (i.e. the market split by where design and purchasing decisions are made). In this way, the influence of sales determined by overseas design groups is eliminated, and the figures better represent the adoption of the technology by local design teams. This leads to the distribution shown in *Figure 5-4*.

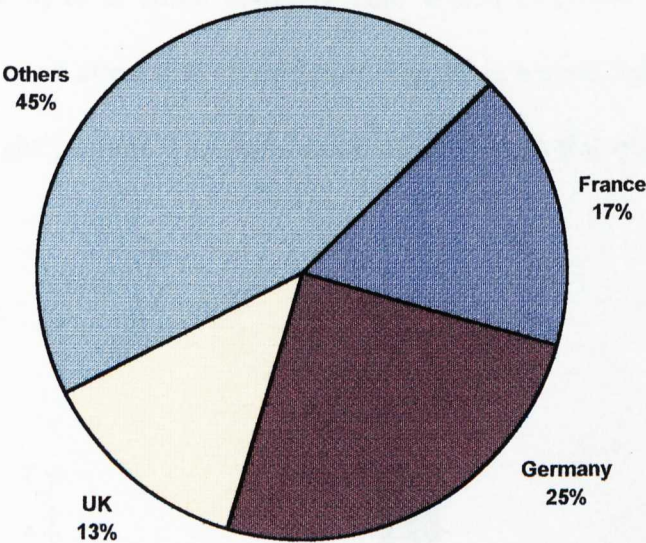


Figure 5-4. European deciders semiconductor market.

Courtois supports his view of France as the emerging champion of the European electronics industry by pointing out that in 1991, the French TTL market plunged by 40% while its ASIC market grew by 20%, suggesting a shift to higher levels of integration in the electronic products produced in French factories. If this perception is correct, it supports the view that the UK is falling behind its overseas competitors.

5.4 The masked ASIC market.

5.4.1 UK Masked ASIC market

Most respondents to the supplier questionnaire considered that the total number of masked ASIC design starts in the UK was in the range of 100-200 per year. However, when the sum of all of the design starts claimed by each respondent were added, it came to about 400. Clearly there is some disparity here which is probably due to over-claiming by respondents in an attempt to show their company in a good light. It may also mean that the market is slightly larger. The distribution of answers to this question is shown in *Figure 5-5*.

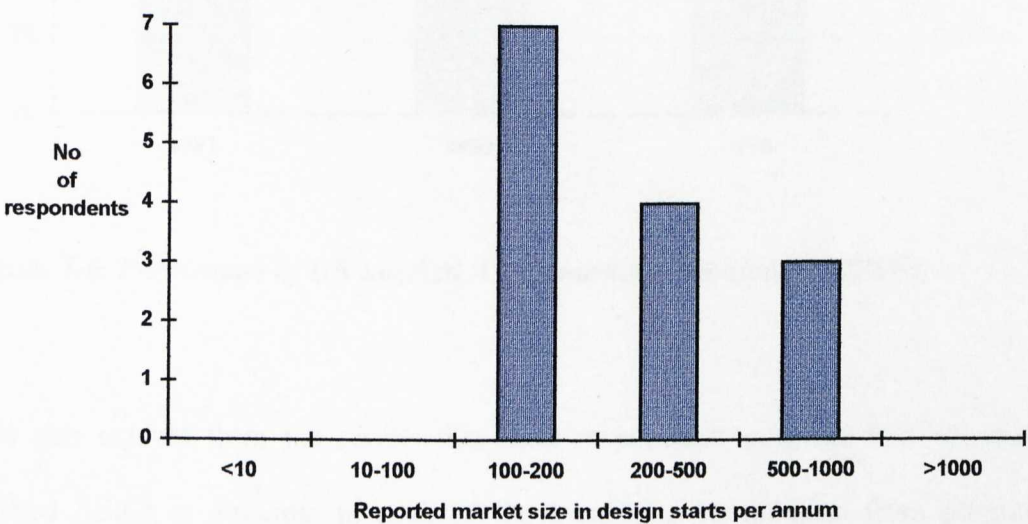


Figure 5-5. Perceived masked ASIC market size reported by suppliers

The proportion of that market attributable to SMEs is somewhat more difficult to ascertain, and needs to be inferred from the questionnaire responses. Some companies replied in percentages, while others gave actual results, but when correlated, it seems that

SMEs accounted for around 8-10% (*Figure 5-6*) of the total number of design starts. In round figures, this amounted to about 20 design starts per year in 1993. It would appear that this percentage may be growing slightly due to the specific efforts of companies who aim their marketing effort at small enterprises, but this effect accounts for no more than about 5 extra designs each year. When semiconductor vendors were informally questioned early in 1997, it appeared that the situation had not significantly altered.

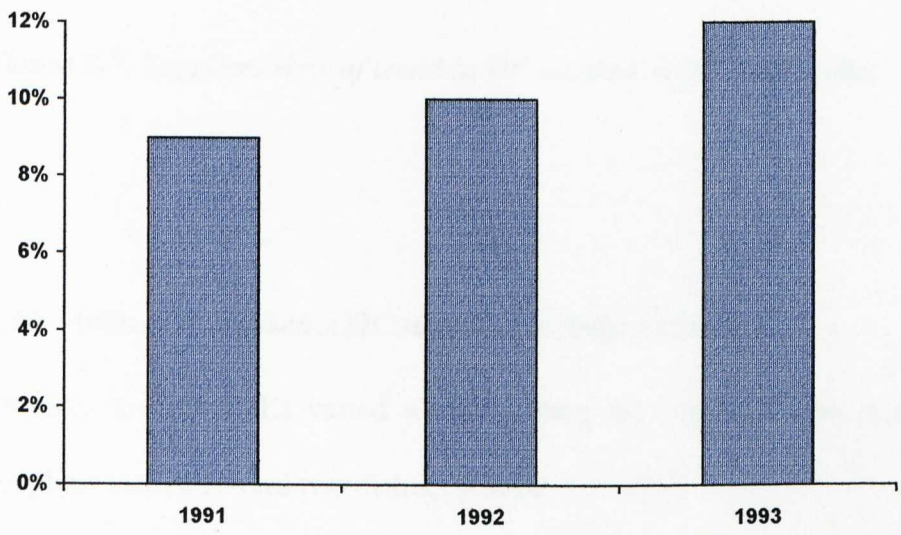


Figure 5-6. Percentage of UK masked ASIC market attributable to SMEs.

It is also evident from the results that most respondents consider that the market for masked ASICs is growing, in spite of the increasing competition from programmable devices. The result of this question is summarised in *Figure 5-7*.

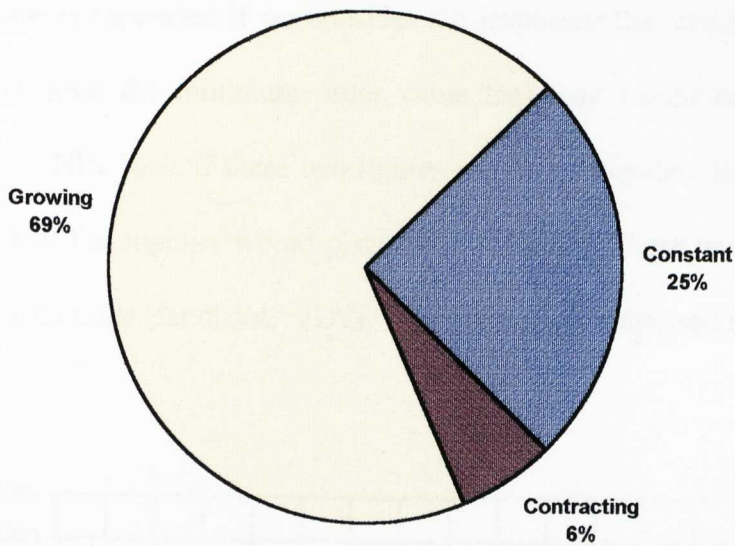


Figure 5-7. Suppliers view of trend in UK masked ASIC market size.

5.4.2 Attitude of masked ASIC suppliers to SME customers.

Attitudes toward SMEs varied widely among the suppliers who replied to the survey. Suppliers tended toward two distinct groups.

The first group of suppliers specifically target SMEs and rate the technical and commercial ability of those SMEs highly. These suppliers tend to be companies that are structured to support SMEs with, for example, multi-project wafers, and so are able to generate sufficient revenues from low volume supply to justify their activity in the SME market.

The second group consists mainly of large, high-volume semiconductor suppliers who, although willing to accept business capable of sustaining sales revenues in excess of £200k per annum (off the record quote from a major semiconductor company), have neither the equipment nor the company structure to support lower volume users.

This view is supported if we consider the responses that companies gave when asked by the DTI what the minimum order value that they would accept was, and what their minimum NRE was. If these two figures are added together, the total represents the entry hurdle that the supplier would place on a customer. These values are given in the DTI's 'Custom Circuits Handbook' (DTI, 1994) and are summarised in *Figure 5-8*.

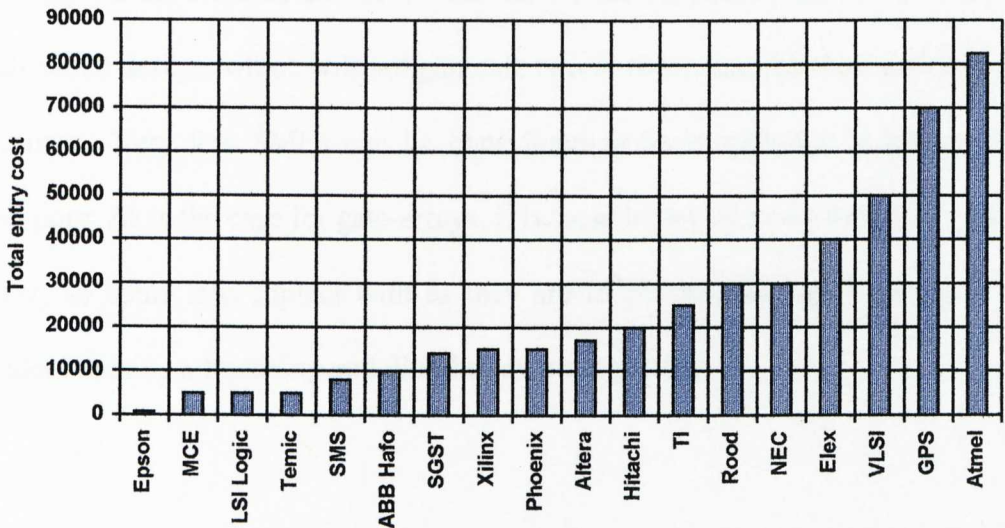


Figure 5-8. Total entry costs - Mask programmed gate arrays.

It can be seen that, for mask-programmed gate-arrays, a number of low-volume suppliers exist who are prepared to offer total entry costs below £20,000. After this point, the minimum entry costs rise significantly as we begin to encounter large semiconductor companies whose high-volume fabrication facilities are not suited to low-volume production. At the extreme end we see a number of companies who are simply saying, 'Don't come to us with anything but a very high volume design'. Clearly, new entrants and SMEs are generally going to be put off by entry costs of over £50,000 for gate-array products, unless they can be very sure of the potential for their proposed product. It is not surprising, given some of these figures, that new entrants see cost of entry as a significant

hurdle, particularly when one considers that it is the large and expensive companies that users are more likely to come into contact with through distributors and advertisements.

The situation becomes even more polarised when the same figures are calculated for cell-based ICs (Figure 5-9). A number of low-volume/low-cost suppliers still exist. Again these are generally companies that take specific steps to reduce entry costs (e.g. multi-project wafers). At the extreme end of the market we see suppliers who do not wish to consider cell-based designs which will not generate two to three hundred thousand pounds worth of business. Very few SMEs can be considered to have applications which fall into this category. As is the case for gate-arrays, it is these high-cost companies that SMEs are most likely to come into contact with as they are in general the larger companies who have wider reaching advertising and distribution arrangements.

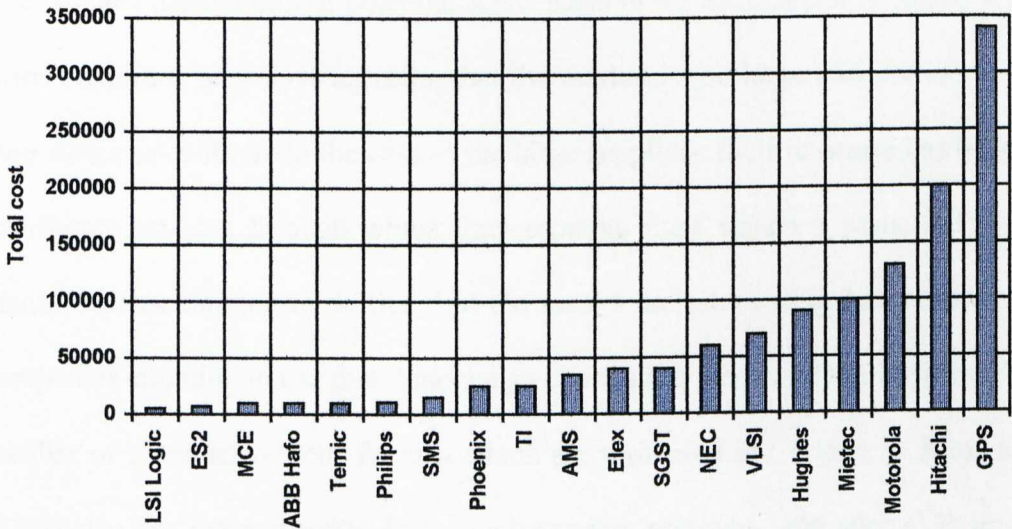


Figure 5-9. Total entry costs - cell based ICs.

5.4.3 Attitudes expressed in the supplier survey.

The attitude questions of the survey lead to a number of conclusions regarding the way ASIC supply companies view SME users. The replies are again slightly contradictory in some areas and suggest that the market is not fully understood, even by companies operating in it.

Half of the respondents (50%) agree that, ‘many of our customers are SMEs’. However, the distribution of responses is significant. The companies that disagree consist mainly of the ones who are identified above as having very high entry-level costs (e.g. GPS, SGST, NEC). Companies who claim to have a high proportion of SME customers seem to be the ones who claim to have low entry-level costs and specific marketing initiatives aimed at low-volume users (e.g. VLSI, MCE, ES2, Semefab).

The size and distribution of potential ASIC users in the SME sector is clearly a problem to ASIC suppliers, with 75% agreeing that the market is too large and diverse to cover with their direct sales force. In the case of the large suppliers, their response has been to use the distributor network through which they promote their standard parts. All of the major manufacturers claimed to do this, but the results do not seem to have been good, as the companies claiming to use distributors also claim a low level of SME business. There are a number of potential reasons for this which are discussed in *Chapter 6*. Most respondents (73%) also use indirect methods (e.g. advertising, seminars, and shows) in an attempt to identify SME clients.

Attitudes to the ability of SMEs to successfully implement ASIC are also widely spread but polarised, with 50% of respondents agreeing that small companies are fully capable of

ASIC design. Again, it is the large suppliers who feel that SMEs are not fully capable of ASIC design, while the low-volume suppliers believe that they are. In addition, suppliers of analogue ASICs are also critical of SMEs' capability. This is probably due to the increased complexity involved in such designs which make them inadvisable to the inexperienced designer. When the question is phrased in terms of engineers' capability, only 31% (again mainly the majors) feel that the inability is an engineering one.

The same polarisation appears with regard to sales volumes. Fifty percent of respondents believed that SMEs have sales volumes that justify ASIC implementations, with most of those disagreeing coming from the large suppliers. As some of these large suppliers also have the highest entry and minimum order costs this is of little surprise. Clearly, volumes have to be much higher to amortise successfully over a high NRE than they do over a low one.

Fifty-six percent of respondents agree that NRE charges and other entry costs (e.g. design tools) form a barrier to adoption of the technology. This group again contains most of the majors, but some of the smaller companies also see this as a problem. It is interesting that this is such a relatively low figure, as cost of entry is the single most important factor identified in any surveys of the potential users. Clearly, some suppliers feel that there are low-cost routes to silicon while users do not.

Most respondents (69%) are in agreement that many successful ASIC designs come from small companies. Again though, these parts do not seem to be being made by companies usually associated with high-volume manufacture in spite of the fact that many such designs are manufactured in high volume.

These responses suggest a two-tier supply industry. The major semiconductor companies are disinterested in SME clients because they do not believe that they have the skills, sales-volume or necessary capital to use ASIC devices successfully in their products. On the other hand, the smaller suppliers and those large suppliers who specifically target SMEs have seen some success. They believe that the SME user is fully capable of designing and profiting from the use of ASIC technology. The reasons for this polarisation of perceptions should be investigated.

5.4.4 The European mask-based ASIC market.

The position of the UK in ASIC consumption has changed in the last few years. According to Dataquest (Ivey, 1994) only a few years ago the UK led Europe in its consumption of ASIC devices, but the recent Dataquest surveys suggest that the UK has slipped into second place behind Germany. The European ASIC market ranked by revenue is summarised in *Figure 5-10* below (Ivey, 1994). In considering the UK position, the predominance of overseas ownership in the UK electronics industry must also be considered. This was discussed earlier, when the total European semiconductor market was considered.

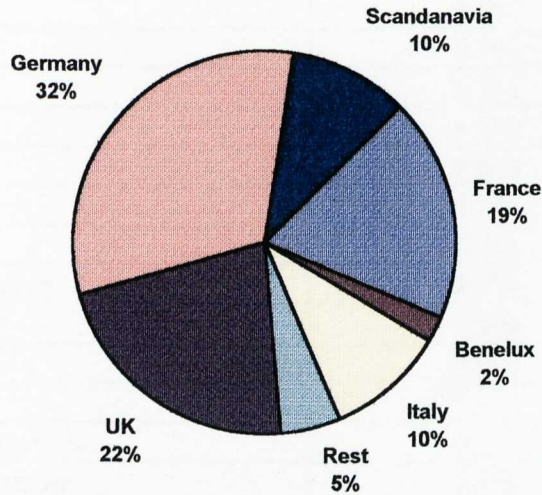


Figure 5-10. European masked ASIC market 1994.

The Dataquest survey suggests that the UK will maintain its market position in a market that is predicted to grow by a factor of two between 1994 and 1999. This supports the results of the survey performed for this study which suggested a growing market, but also suggests that the UK is starting to slip behind its European competitors in the use of this technology.

5.4.5 Masked ASIC market share in Europe.

According to Dataquest the European ASIC market in 1991 was segmented by revenue as shown in *Table 5-2*.

Supplier	Market share
GEC Plessey	8.9%
LSI Logic	6.7%
Mietec	6.7%
Siemens	6.7%
Texas Instruments	6.6%
SGS-Thomson	4.7%
Toshiba	4.4%
Austria Mikro Systeme	3.9%
VLSI Technology	3.8%
Motorola	3.4%
NEC	3.4%
Advanced Micro Devices	3.2%
National Semiconductor	3.1%
Philips	2.6%
AT&T	2.0%
ES2	1.9%
Matra-MHS	1.9%
Fujitsu	1.8%
Harris	1.8%
Xilinx	1.8%

Table 5-2. European ASIC market share.

In general, these figures agree with those reported by companies in the supplier survey when extrapolated for all of Europe and so help to confirm the validity of those figures (e.g. GPS 9% market share would suggest a 1000-2000 design start market size in Europe, which agrees with EU estimates).

5.4.6 Masked ASIC design-starts worldwide.

According to Dataquest (reported in *Atmel News*, Feb 1996), the geographical distribution of masked ASIC design-starts in 1995 is as shown in *Figure 5-11*. These figures tend to agree in broad terms with those ascertained elsewhere for the UK and European cases and so serves to support the conclusions regarding the UK market made elsewhere in this study. One interesting observation is the extent to which Europe is significantly behind both the USA and Japan in design starts.

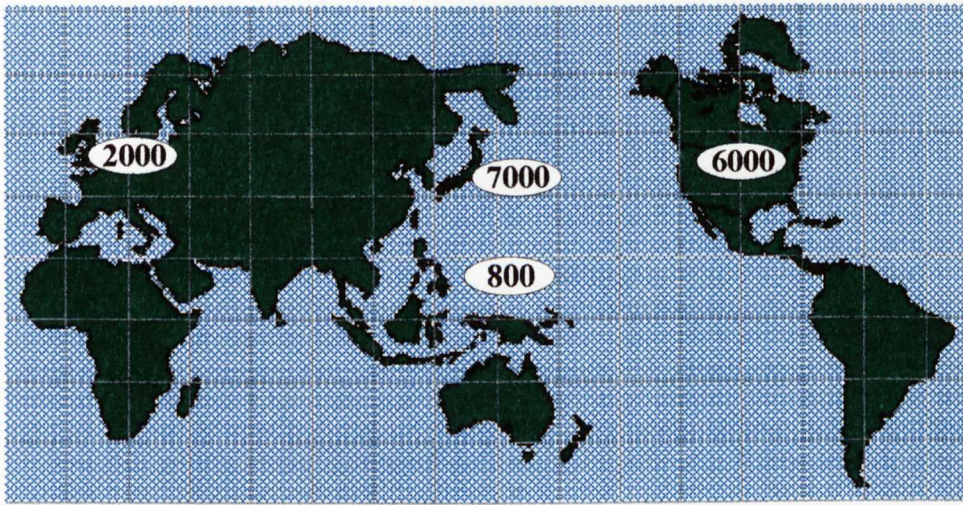


Figure 5-11. ASIC design starts. World map

These figures lead one to believe that adoption in Europe has fallen significantly behind that of its major trading rivals (USA, Japan and the Pacific Rim), particularly as the figures refer to design starts rather than volume consumption, and so remove the effect of ‘screwdriver plants’ set up simply to take advantage of low-cost local labour.

5.5 The Programmable-logic market.

One of the most important developments to influence the ASIC market in recent years has been the introduction of the Field Programmable Gate Array (FPGA). In 1984, Ross Freeman, then employed by Zilog, left the company, patented the concept of a reprogrammable logic element and set up Xilinx to develop and exploit the technology. Since then the company has grown to a turnover of \$256million in 1994. This represents 25% of a \$1billion FPGA market which is expected to grow to \$2billion by 1997. (Manners, 1994). Similarly, *Electronic Times* reported in early 1994 that Actel, the inventors of the Antifuse, saw their 1993 turnover grow by 35% to \$59.6million. (Anon, 1994: 1).

It is predicted that by the year 2000, programmable logic will have risen from its current 8.3% of the CMOS logic market to 25%. This is summarised in *Figure 5-12* (Manners & Parry, 1994).

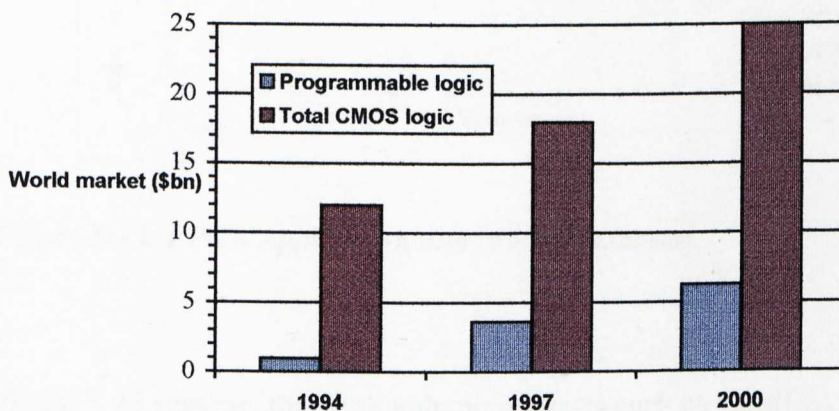


Figure 5-12. Predictions for programmable logic market

This view of increased functionality and lowering cost is supported by Xilinx (Clarke, 1994:1) who see their devices increasing in complexity and coming closer to the prices of masked ASIC devices as the feature-size reduces. Xilinx has positioned the price of its 25,000 gate device (XC4025) at below \$400 in 5000 off volumes in early 1995, with the hardwire equivalent costing around \$40 in high volume. Consequently, they predict the use of their devices to be split across application areas as shown in *Figure 5-13*.

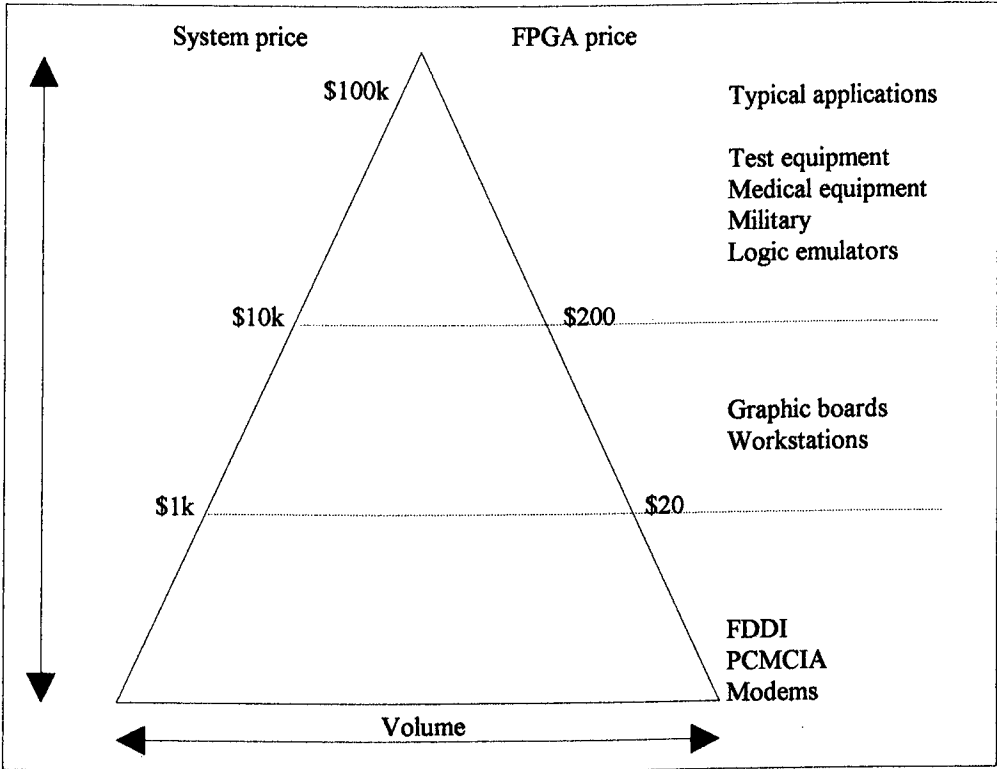


Figure 5-13. FPGA Application and price predictions.

Figure 5-13 suggests that high-volume products such as PCMCIA cards and modems, with production volumes of hundreds of thousands of units and a system cost of less than

\$1000, can tolerate FPGA prices of up to \$20. Low-volume, high-value equipment with system costs approaching \$100,000 is expected to tolerate FPGA prices in excess of \$200.

5.5.1 FPGA suppliers market shares.

Three main suppliers of FPGA devices (Xilinx, Actel and Altera) initially emerged with the introduction of the technology to the market in the 1980s. A number of minor suppliers also emerged, sometimes to be absorbed by the larger players (e.g. Quicklogic). By 1991, the FPGA market was estimated to have been split as shown in *Figure 5-14* (Courtois, 1994).

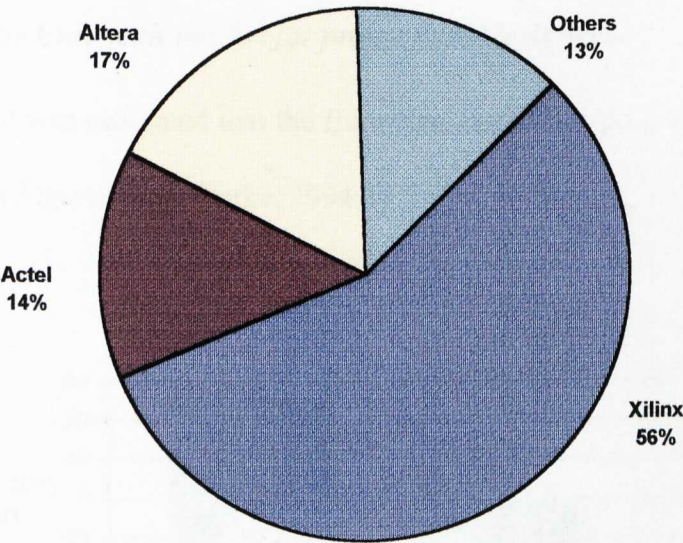


Figure 5-14. FPGA market share in 1991

By 1995, according to the market research company Integrated Circuit Engineering (ICE, 1994) the position had changed somewhat with a number of acquisitions, mergers and new entrants. This is summarised in *Figure 5-15*.

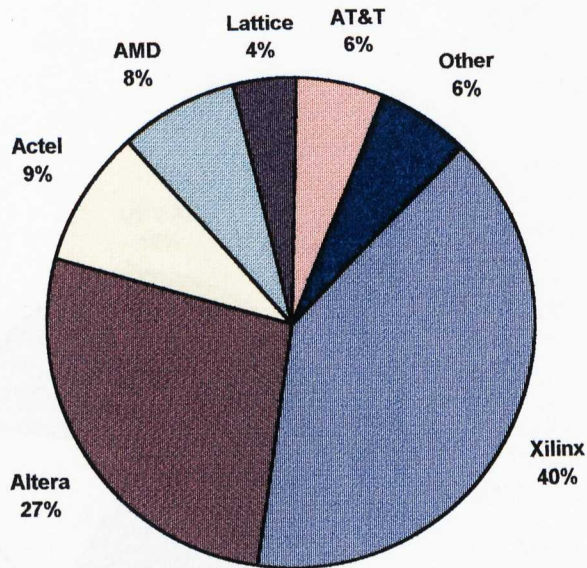


Figure 5-15. High density PLD market share in 1995.

5.5.2 The European market for programmable devices.

In 1994 it was estimated that the European market for programmable logic devices was as shown in *Figure 5-16* (Clarke, 1994:1).

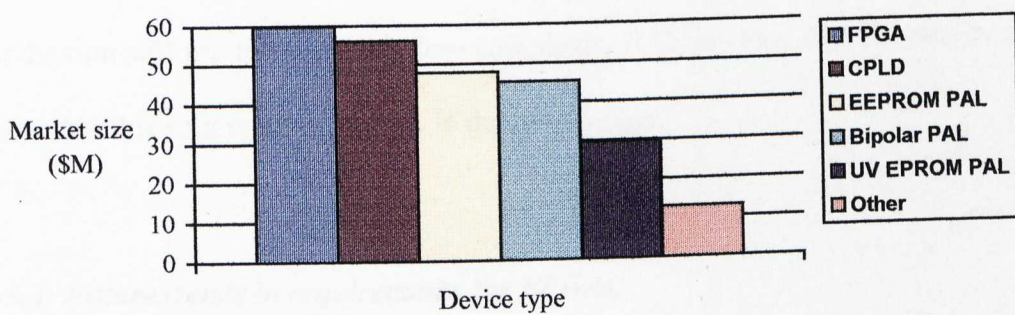


Figure 5-16. European programmable logic market by type.

The market segmentation between the different types of programmable logic is shown in *Figure 5-17*.

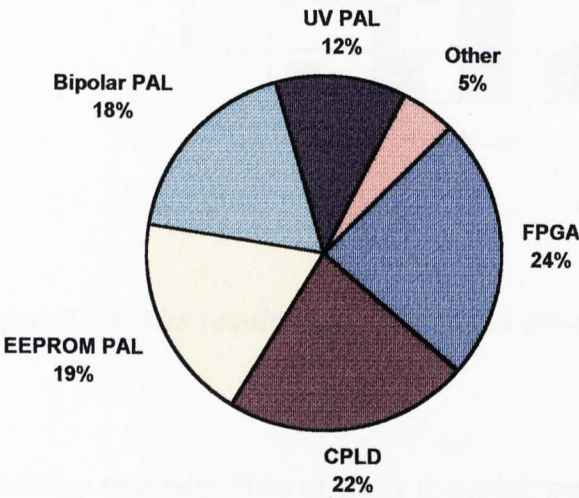


Figure 5-17. European market for different programmable technologies

As most of the ‘other’ category above relates to development systems, it can be seen that there is an approximately even split between FPGA/CPLD with 46% of the market and PAL devices of varying types which have 49%. Clearly, many designs currently in production still use the relatively low-complexity PAL devices. But the survey went on to show that this split is set to change in the near future.

5.5.3 Future trends in requirements for FPGAs.

The IMS survey previously cited (Clarke, 1994:2) also reviewed the requirement for gate density in future FPGA designs, and gives some useful evidence into the way in which this technology will encroach onto the ground previously held by masked gate-arrays. The findings of the survey are summarised in *Figure 5-18*.

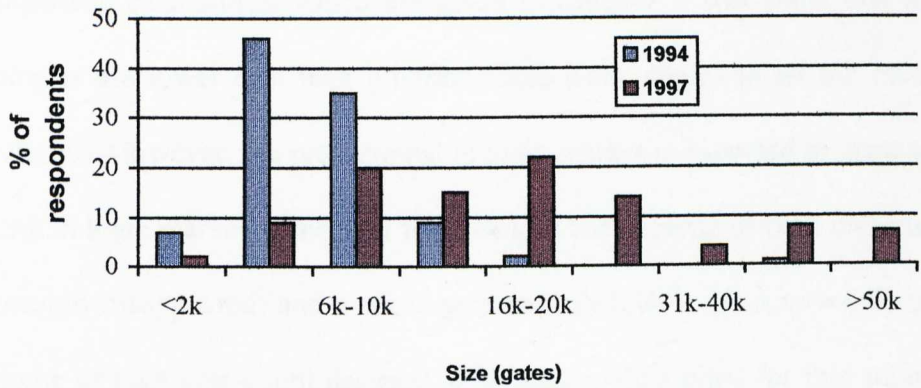


Figure 5-18. Size requirements for FPGA 1994-97.

It follows that with 50% of users requiring gate-counts of 16,000 and above, that firstly the FPGA manufacturers must continue to develop denser arrays, and secondly that the lower end of the traditional gate array market (5-20k gates) will be severely eroded by FPGA products should they become available at competitive prices.

5.5.4 Reasons for the growth in programmable logic

The cost comparison calculations which are given in *Chapter 7* will show that masked ASIC technologies are lower cost than programmable technologies in all but fairly low production volumes. However, the programmable logic market is expected to grow to over 25% of the CMOS logic market in the next few years, at the expense of both discrete logic (which has virtually disappeared) and masked gate-array (which is often now only used in very high-volume or high gate-count designs). One reason often cited for this anomaly is ‘time to market’. One model that clearly shows the effect of time to market is set out in *Figure 5-19*. This model, generally attributed to Logic Automation Ltd, considers the life-cycle of a product. Although generally considered to be a normal curve, the revenue generated by a product over time can be approximated to the triangle shown in the figure. The outer triangle shows the maximum revenue available from a particular product, while the inner (yellow) triangle shows the effect of delaying the product introduction by a delay time (D).

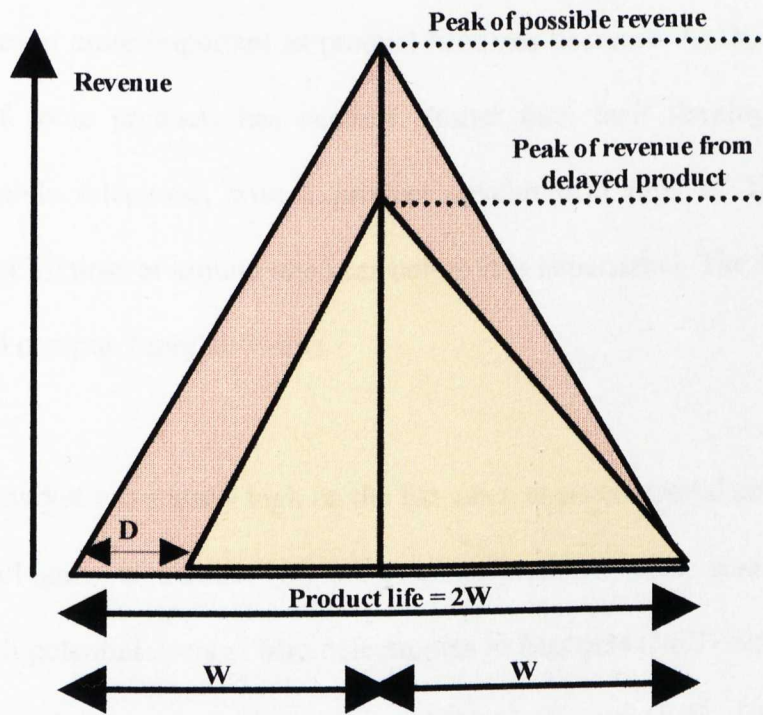


Figure 5-19. Delayed market entry model

Lost revenue, expressed as a percentage of total possible revenue, caused by a delayed product introduction can thus be shown to be:

$$\text{Lost Revenue} = D((3W-D)/(2W^2)) * 100$$

For a selection of projects, this equates to the figures shown in *Table 5-2*.

Target revenue (£K)	Product lifetime	Lost revenue (£K) due to delay of :		
		1 month	2 months	3 months
300	36 months	25	48	71
300	18 months	48	93	133
200	36 months	16	32	47
200	18 months	32	62	89
50	36 months	4	8	19
50	18 months	8	15	22

Table 5-3. Revenue loss due to late market entry

While it might be possible to question some of the assumptions made in generating the model, the fact remains that ‘time to market’ must be seen as a major development driver. This becomes even more important as product lifetimes decrease. At the time of writing, the lifetime of some products has become shorter than their development time. For example, a mobile telephone, with a product development time of 18 months has a realistic product lifetime of around one year before it is superseded. The same is probably true of personal computer motherboards.

While time to market was clearly high on the list when users compared programmable and masked technologies, a number of other considerations were also evident. From discussions with potential users at Microelectronics in Business (MiB) seminars, and from opinions expressed in the trade-press and published surveys (ICE, 1994) the relative advantages of each technology are seen as those shown in *Table 5-4*.

User programmable logic advantages	Mask programmed logic advantages
No NRE	Higher density
Easy second sourcing	Higher volume at economic price
Lower volume purchase possible	Higher performance (speed/power)
Redesign easy and painless	Macros available
In-system reprogrammability	

Table 5-4. UPD Vs Mask programmed devices

5.6 The microcontroller market.

5.6.1 The world microcontroller market.

Early in 1994, *Electronics Times* reported on a survey performed by Frost and Sullivan (Anon, 1994:3) which suggested that the trends in the world market for embedded microcontrollers are as shown in *Figure 5-20*.

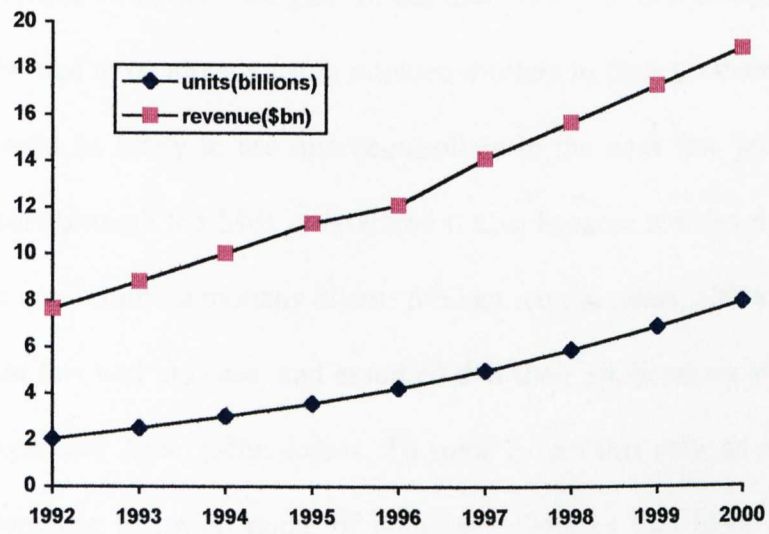


Figure 5-20. World embedded controller market. 1992-2000

5.6.2 The UK microcontroller market.

In summer 1994, the trade magazine *Components in Electronics* conducted a survey into the use of microcontrollers in the UK (Anon, 1994:2) and found, perhaps surprisingly, that while Intel held the greatest market share (19.6% by respondent), second place went narrowly to Arizona Microchip (18.8%). Motorola came third with 16.1 % while others including Hitachi, Philips, and NEC also featured. Sixty seven percent of respondents

claimed to be using 8-bit devices, and 24% to be using 16-bit. It is interesting to note that Waterside Ltd (see case studies in *Chapter 3*) managed to make a significant cost saving using a small microcontroller device in a simple control application. The high uptake of the Arizona Microchip parts suggests that a large number of other such low-complexity applications may also exist.

It would appear that the uptake of microcontroller technology is far higher than the uptake of other ASIC technologies. In the user-survey of this study, 18% of companies surveyed claimed to be already using microcontrollers in their products, and 38% claimed that they would be likely to use microcontrollers in the next few years. In contact with potential users through the MiB programme it also became evident that microcontrollers provided an ideal solution to many clients product requirements, although many users were unaware that this was the case, and assumed that their applications would require the use of more expensive ASIC technologies. To some extent this reflects a failure of potential users to recognise the wide range of additional features that have become available on simple microcontrollers in recent years, or to recognise the significant reduction in price that has taken place in the same period.

5.6.3 The European microcontroller market.

According to Miller-Freeman (Anon, 1996) the European microcontroller market in 1997 was predicted to be as shown in Figure 5-21.

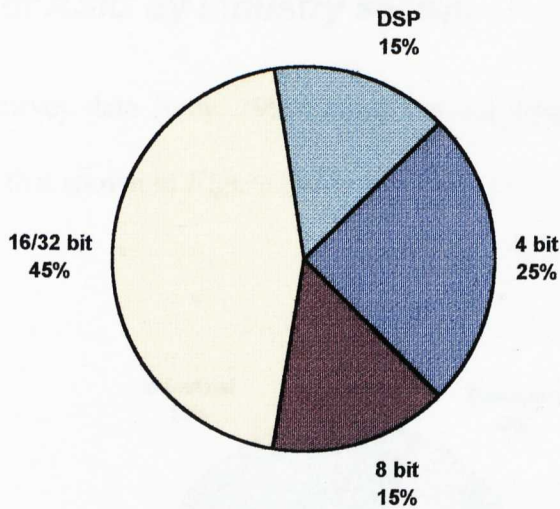


Figure 5-21. European microcontroller market in 1997

By 1997, the total European market for microcontrollers is expected to be \$3billion, compared with \$1.2billion in 1992. The predominant technology is expected to become 16/32 bit devices, as they reduce in price due to the demands of the mobile communications market. Significantly, four-bit devices are still expected to have a major role (25% of the market). This requirement for very simple low-cost devices will be driven by low complexity consumer applications.

5.7 Use of ASIC by industry sector.

Dataquest survey data (Ivey, 1994) considers the usage of ASIC technology by industry sector to be that shown in *Figure 5-22*.

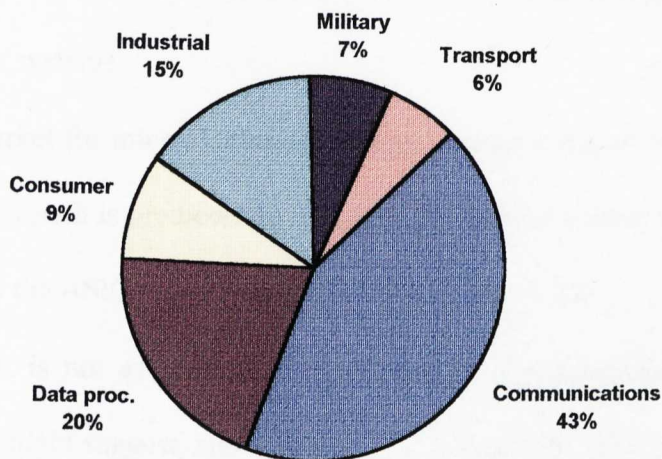


Figure 5-22. World ASIC consumption by product area.

The world's largest user of ASIC technology is the communications industry, where the size, weight and power consumption requirements for portable equipment have been met by CMOS ASIC devices. This market continues to drive ASIC technology to lower voltage, higher complexity devices as more sophisticated digital radio telecommunications systems such as the Global System for Mobile Communications (GSM) emerge. In contrast, consumer products account for a relatively small percentage of the total (9%), implying that they only use ASIC devices in a very small number of possible applications (greater adoption would swamp the statistics due to the high volumes in which consumer products are sold). As these statistics relate to the world market, it would seem that the UK is not alone in missing the potential of the technology.

5.8 Conclusions on the ASIC market

The information included in this chapter leads to a number of conclusions regarding the nature of the national and international ASIC markets:

- A diverse system of large and small companies exist in both the supply and user side of the industry, and they form a complex system which is highly interactive with a number of other systems
- The market for microelectronic devices is large and growing at a spectacular rate. This rate of growth is predicted to continue for the foreseeable future. The growth is evident in all of the ASIC technologies discussed in this study
- The UK is not as prominent in its use of microelectronics as its raw consumption figures might suggest, and appears to be falling behind its overseas competitors in some areas. It would appear that as few as 20 masked ASIC designs may be attributed to UK SMEs in any one year.
- Programmable devices and microcontrollers are becoming increasingly important, particularly to SME users, and may be starting to erode some areas traditionally associated with masked ASIC products

6. Analysis of the UK ASIC supply industry and its customers.

This chapter investigates the structure of the UK ASIC supply industry in relation to the market that it serves.

6.1 The Porter industry forces model.

In analysing the information given in *Chapter 5* it is useful to consider the UK supply industry in relation to the model developed by Michael Porter (Porter, 1979).

Porter states that an industry may be analysed by considering a number of significant forces (such as the threats of new entrants and substitute products) and by considering the relative strengths of suppliers and buyers operating in the industry. This is summarised in *Figure 6-1*.

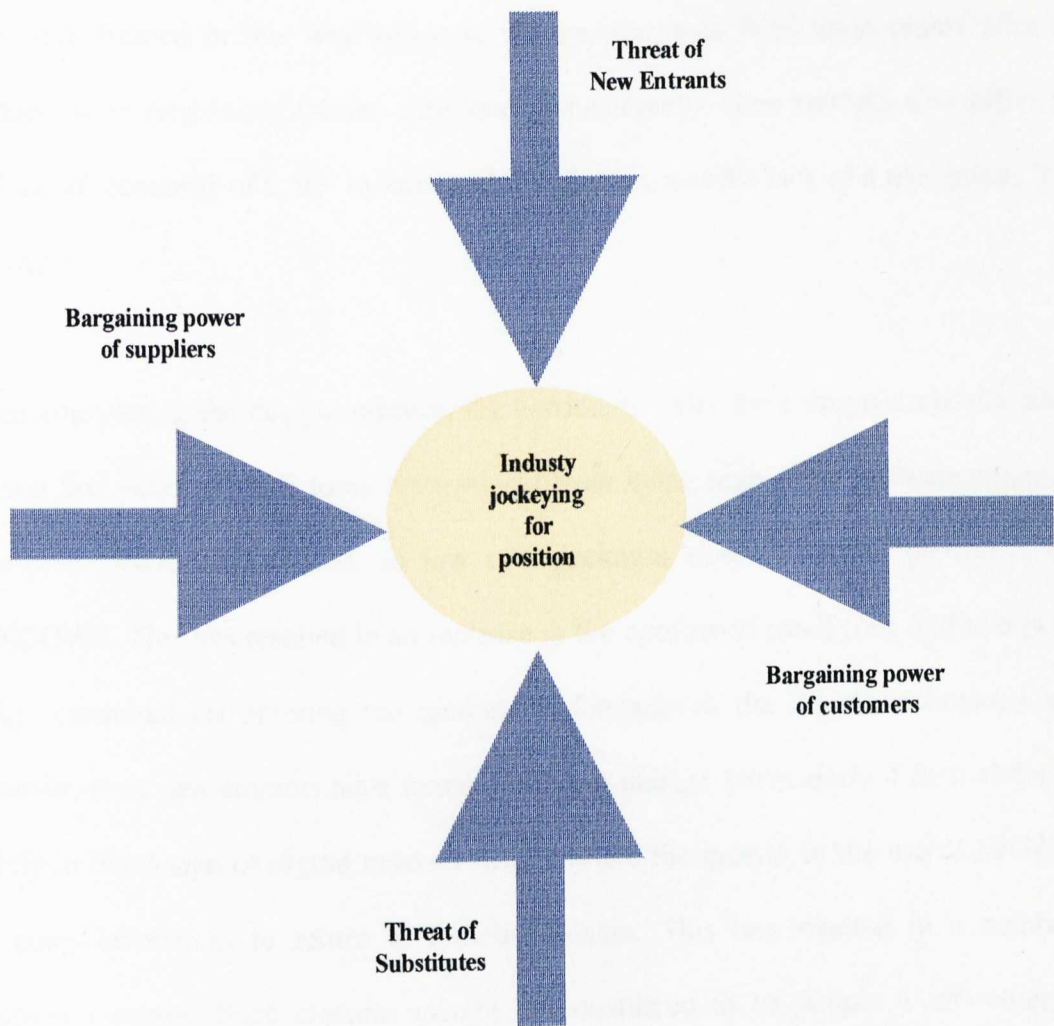


Figure 6-1 How competitive forces shape strategy.

6.1.1 Threat of new entrants.

It is generally considered that there is little threat from new entrants to the semiconductor manufacturing industry because the barriers to entry are so great. The entry costs involved in setting up a chip fabrication plant run into hundreds of millions of pounds and have generally only been achieved with a high degree of government support. Exceptions have included the so called 'fab-less chip manufacturers' who have designed products which they then have manufactured by a chip foundry (generally one of the large semiconductor companies). This helps to overcome some of the entry barriers, although not the costs of initial design and marketing of the new products. Some of the recent FPGA companies

have been formed in this way and only set up their own fabrication plants after their products were established (Xilinx falls into this category). New entrants also suffer from the lack of 'economy of scale' in sales and distribution, and the lack of a recognised 'brand identity'.

When considering the design industry, the barriers to entry have dropped considerably in the last few years as CAE tools have moved from being high-value software running on expensive UNIX workstations, to low cost packages running on PC platforms under WINDOWS. This has resulted in an increase in the number of small (one and two person) design consultancies entering the market, particularly in the digital technology areas. However, such new entrants have found a difficult market, particularly if their skills were mainly in the design of digital masked ASICs where the growth in the use of FPGAs has led many companies to return to in-house design. This has resulted in a number of company closures. Such closures cannot be considered to be simply a reflection of a general economic downturn as other design companies, offering a wider range of more specialised services (e.g. analogue or R.F. design), have flourished during the same period. This would tend to support Porter's view that lowering entry barriers allow additional companies to enter the market and compete, but the consequent increase in price competition results in a volatile market with frequent company failures.

6.1.2 Powerful suppliers and buyers.

Suppliers can be considered to be powerful in an industry if they are few and more concentrated than the industry itself, or if they provide unique or highly differentiated materials. This was seen to be the case in the microelectronics industry when the Japanese plant which produces much of the world's plastic chip encapsulation material burned

down. The resultant lack of material caused a shortage of semiconductors for a short period of time, and a consequent increase in price.

Although some buyers of semiconductors may be considered to be powerful due to the large volumes that they purchase (e.g. major computer suppliers buying DRAM), this cannot be said to be the case with SMEs buying ASICs. In general, some 'shopping around' may be done before the design is begun, and consequently NREs may be driven down but, once the chip is designed, the high cost and subsequent risk of moving production to another supplier means that it is rarely (if ever) done. In consequence, the SME may see itself as being at the mercy of the semiconductor vendor. The lack of a second source was seen as a major barrier to entry by respondents to the DTI survey of 1991 (Shortland, 1991) but was not specifically identified in the survey performed for this study in 1994/95.

6.1.3 Substitute products.

The threat of substitute products have had a considerable effect on the ASIC supply industry. The perceptions of high cost, risk and other factors have long led potential users to stick with proven, non-integrated solutions. In more recent times, the higher complexity available in FPGA products has significantly eroded the market for low-end masked digital ASICs. This has led to a number of established ASIC design and supply companies closing or drastically reducing their gate-array support activities (e.g. LSI Logic reduced the size of its UK support centre, Texas Instruments closed its UK facility at Bedford, centralising ASIC support for Europe in France, and a number of design consultancies set up solely to do ASIC design have been forced to close (e.g. Array Consultants)). In ASIC design, individual subcontractors, brought onto a company's internal design-team specifically for

an individual ASIC design have become more attractive than using an external consultancy as the cost of design tools has fallen. The role of design consultancies and sub-contractors is discussed in more detail later in this chapter.

6.1.4 Internal jockeying for position.

Product differentiation and a drive to reduce prices are often seen as major forces involved in internal industry competition. A lack of product differentiation has led to considerable changes in the masked ASIC industry. In the mid 80s, when a large number of applications could be found for the largest ASICs available (around 5000 gates) the company that had the largest devices could differentiate their product and charge premium prices. However, in the late 80s, as gate counts reached 100,000 and above, fewer and fewer applications requiring such complexity could be identified. Even today, most applications remain below 50,000 gates. As most suppliers can now produce these devices, price becomes the major difference between suppliers. Unfortunately, the companies that previously enjoyed premium pricing were not structured for price competition, having large support and sales organisations. Such companies have suffered severely.

6.2 Market maturity.

When one considers the results of the initial DTI survey (Shortland, 1991) and the results of the supplier questionnaire performed for this research it is possible to draw some conclusions regarding the maturity of the UK ASIC market.

6.2.1 A model of market maturity.

Market maturity can be expressed in terms of the type of user that has already adopted a new product (Spence, 1994). The number of users adopting a product over time can be assumed to show a normal distribution, and by segmenting the distribution it is possible to categorise the type of adopter most likely to be active at any point in the adoption life-cycle. These categories of adopter are classified as Innovators, Early Adopters, Early Majority, Late Majority and Laggards. This model is shown in *Figure 6-2*.

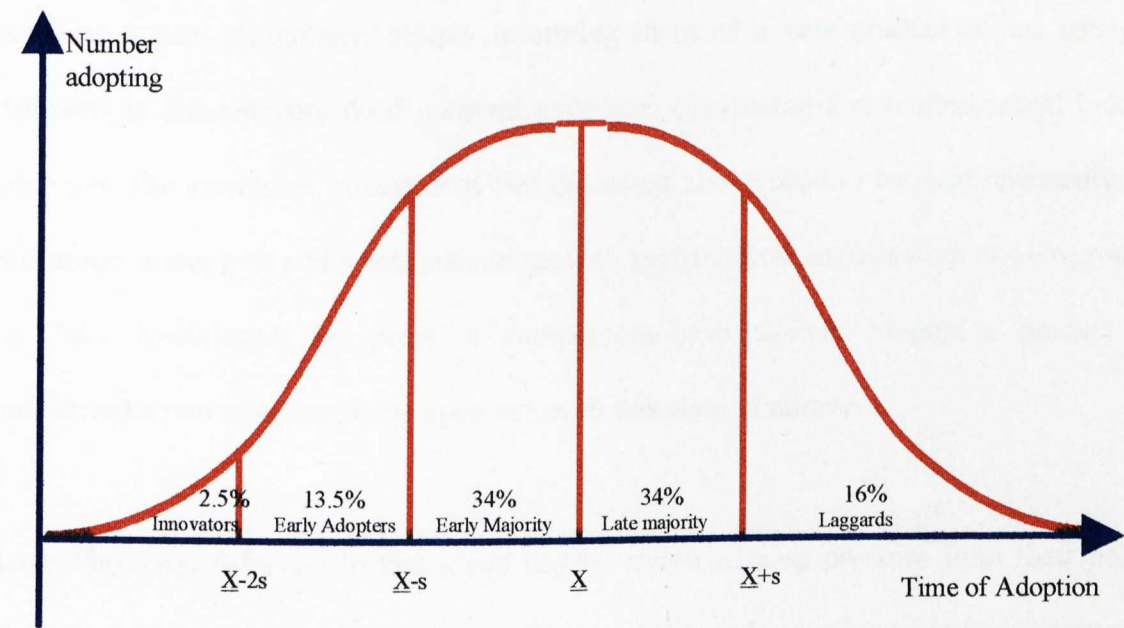


Figure 6-2. A model for adoption

Spence maintains that adoption characteristics of the groups can be described as:-

Innovators. The first people to adopt a new process. These people are generally more venturesome than the norm and need little persuasion to adopt. The most effective means of marketing therefore is simply awareness raising. This might typically be done by advertising or mail-shots.

Early Adopters. These people are marginally more cautious than innovators, though still significantly ahead of the average. This group often act as 'legitimizers' to the larger group, convincing them that adoption is worthwhile because they are seen as more cautious than the innovators. Awareness raising activities such as advertising and mail-shots would typically be augmented with activities such as seminars and product trials.

Early Majority. This group, not being noted as innovators, are exceedingly deliberative in adopting a new technology. Simply informing them of a new product is not enough. Adopters in this category need constant exposure, convincing and reinforcement before adoption. The awareness raising activities discussed above need to be used repeatedly on this group, along with additional encouragement, perhaps from membership of user-groups or clubs. Knowledge that peers or competitors have already adopted a product is considered a powerful marketing approach with this class of adopter.

Late Majority. Adopters in this group require overwhelming pressure from their peers before adopting a new product, and even then are likely to be ponderous in their approach. In addition to all of the approaches discussed above, exposure to specific examples of competitors successfully using a technology can be a powerful tool in persuading this group to adopt a new product or technology.

Laggards. This group is generally openly hostile to change and includes the ‘rejecters’ group which will never adopt a new product, but which forms part of the potential market.

This model is useful in considering the adoption of ASIC in the UK but does have some drawbacks. Primarily, it makes the assumption that there is one ‘market’ and one ‘product’. In the case of this research, we are considering a range of products (from programmable logic to masked ASIC) and a market that can be segmented in a number of different ways (e.g. by industry sector or by company size). Consequently, to say, for example, that the UK ASIC market is in the ‘Early Adopter’ phase would be an oversimplification. It is clear that some market segments are more advanced than others. For example, telecommunications companies, whether large or small, have been using ASICs for a number of years and can be considered to show most of the characteristics of a market with new adopters falling in the ‘Late Majority’ phase. A subjective classification of some other market segments is given in *Table 6-1*.

Innovator Phase	Early Adopter Phase	Early Majority Phase	Late Majority Phase	Laggards Phase
Hydraulic Control	Domestic heating	Automotive	Telecom switches	Computers
Medical imaging	Domestic security			Mobile phones
Drug delivery				

Table 6-1. Adoption phase examples

These conclusions would suggest that the UK ASIC market has a number of segments. Some segments, particularly those consisting of larger companies are well down the adoption road and account for the majority of ASIC design-starts each year. The

implication is that marketing to the segments that have yet to adopt ASIC technology will be increasingly difficult. However, it also suggests that a large potential market remains untapped.

Small companies are in general considerably behind the larger ones operating in a particular segment. Clearly, some small companies are using ASICs to produce sustainable competitive advantage (e.g. TRACKER, Waterside and HJ Weir mentioned in *Chapter 3*). But the rate of design-starts compared with the potential market size suggests that most small companies are in the earlier phases of adoption. This has a number of implications both for the ASIC supply industry and for government organisations such as the DTI who are attempting to increase the adoption of the technology through government intervention programmes such as 'Microelectronics in Business'

The implication is that a number of different approaches will need to be applied to address the users at different stages in the adoption process. If all adopters could be assumed to be at the innovator stage, then simple awareness raising activities (such as seminars) might be sufficient to cause adoption, but in the later categories this will not be sufficient. Later adopters will need considerably more exposure and encouragement. The expense of this activity has led some suppliers to concentrate on the innovators, actively avoiding the other groups (off record discussion with major semiconductor company director). While this makes sound business sense for the semiconductor manufacturer concerned, it does little to increase the overall rate of technology adoption.

6.3 The role of distributors and independent design consultancies.

One clear indication from the supplier survey performed for this study was that the large semiconductor manufacturers found it difficult to address a large, disparate market such as the UK manufacturing base using their relatively small direct salesforces. While the major users of ASICs are few and easily identified, potential SME users are difficult to identify and may not initially justify the effort. A number of routes to solve this problem have been investigated.

6.3.1 Distributors design centres.

The first route adopted by some semiconductor vendors was to use the distributors that they use for distribution of their standard parts either simply to identify potential users or to establish design centres to handle turn-key designs which could then be passed to the semiconductor manufacturers for production. On the face of it, this solution appears attractive, but it has been largely unsuccessful for a number of reasons.

Firstly, the salespeople from the distributors generally have little technical training. This is acceptable when selling standard components and dealing mainly with buyers who are interested largely in cost and delivery timescales, but leads to a lack of confidence when the discussion is with engineers who need to feel that their problem is understood by somebody capable of providing a solution. In addition, the time taken to make an ASIC sale is considerably longer than that for standard components, so has a much higher cost associated with it than more lucrative, immediate business.

Secondly, the distribution companies underestimated the technical complexity and investment necessary to provide a high-quality design service, believing the design simply to be a part of a sales process that would quickly bring revenue through supply of the finished component. They severely underestimated both the selling cycle time (from initial contact to design start) and the design and product introduction time that could elapse before a revenue stream from ASIC sales began. These problems are exemplified in the short case study below. It is useful to note that in response to a question in the supplier survey, although 47% of the semiconductor companies claimed to have used distributors in the past, none claimed to have plans to extend this activity in the future.

6.3.2 The XXX Ltd. ASIC disaster.

XXX Ltd. (the company name has been changed for reasons of confidentiality) is a supplier of medium volume products (around 10,000 units per annum) to an industrial market. In their particular market, price is extremely important as product differentiation is difficult. It was an attempt to reduce the cost of the product while also incorporating some new features, that led XXX to consider the use of ASICs.

The company's design team had a great deal of experience of design for their particular market, which was a technically complex one using radio-frequency technology, but they had no experience of ASIC design. They were convinced by a distributor that a mixed-signal, CMOS, standard-cell device met their requirements and that the design of such a chip could be easily performed by the distributor's design centre with little intervention from the company. The company accepted this and ordered the design.

After the company received the fifth iteration of the chip, which still did not work, and the design was running two years behind schedule, it became clear to them that they had chosen the wrong route. At this stage, the author was commissioned to 'trouble shoot' the design and get the product ready for production in as short a time as possible.

There were found to be a number of problems with the circuit-design, the development system, and the project management of the development that could be directly attributed to the choice to use a distributor design centre rather than using internal expertise or a design consultancy.

Firstly, distributors are generally sales based companies, and to be successful in this have a culture based on fast turnover and minimal customer contact (..pile 'em high sell 'em cheap..). This culture does not transfer well to a design environment. A company is far more likely to provide quality of design if design is its major source of revenue. In this case the distributor eventually lost interest in the design and left it to the silicon vendor and XXX Ltd. to sort out the mess generated by their design team.

Secondly, the distributor design centre had chosen to use a design system which was incompatible with that of the silicon vendor who was performing the layout. As a result, layout changes made by the vendor were not fed back to the initial design database which was held by the design centre and in consequence simple connectivity errors were introduced into the design. XXX Ltd would not have taken such a lax approach in its own design work, but assumed that the ASIC 'experts' that they had commissioned knew what they were doing.

Thirdly, an inappropriate silicon vendor was proposed by the distributor. This was because that distributor only represented a single silicon vendor and so proposed them for the development rather than choosing the best supplier for the application. As has been shown by the survey results, two basic groups of vendor exist. The first is only interested in high-volume low-risk business, so is generally the wrong type for a new user who requires engineering assistance and may not have high-volume demands. That assistance is far better given by low-volume suppliers and those who generate revenue through the design process. In this case a supplier from the first group was chosen when one from the second group would have formed a much better fit with XXX Ltd.

In summary, it is useful to review the different roles of the three parties involved in ASIC design (McArdle & Woodley, 1992). This is shown in *Figure 6-3*.

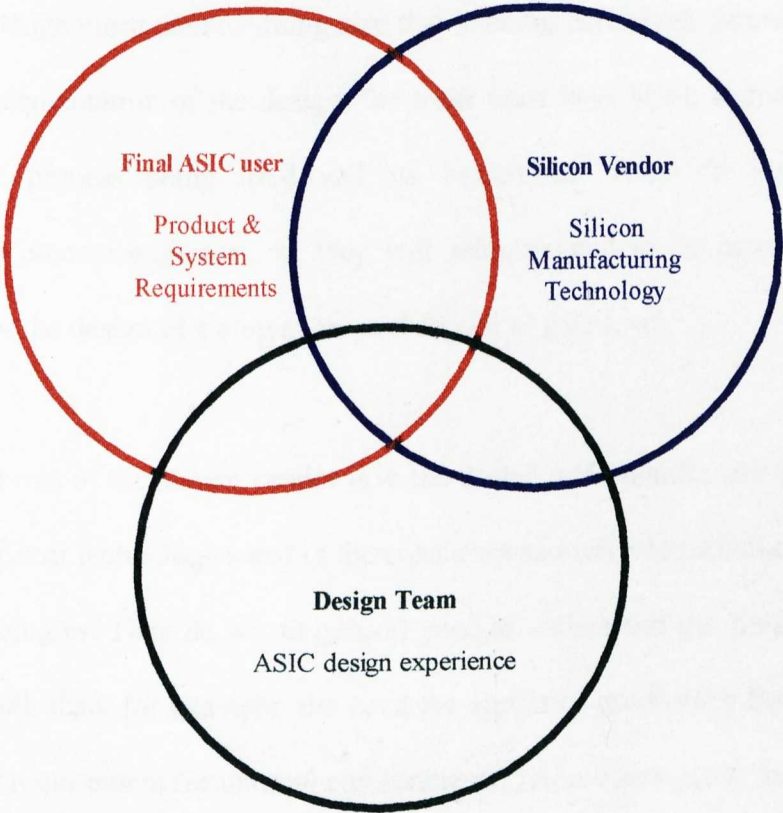


Figure 6-3. Knowledge overlap in the ASIC design process.

The final users of the ASIC need fully to understand and specify the system requirements of the product. They, more than anybody, will know the details of the system in which the device will operate, and the constraints that these place on the operation of the device. This knowledge must either already exist in the design team, or be clearly imparted to them. In discussions with potential users of design services, it became apparent that the failure of consultants to admit that they know less about a client's design requirement than the client himself, which is often seen as arrogance, has led to a client losing confidence in particular consultants. The relationship between the three parties identified in *Figure 6-3* needs to be one of mutual respect and trust.

The design team must be fully conversant with the ASIC design process, and the limits of the particular technology being used in the design. In the case of an external design house, it is this knowledge more than anything else that is being purchased. In order to achieve a successful implementation of the design, the team must have some understanding of the semiconductor process being used and its limitations. They do not need to be semiconductor process engineers, as they will seldom need to be involved in process development or the design of a chip at lower than cell or gate level.

In contrast, the role of the silicon vendor is in the design and manufacture of ever smaller-featured, lower-cost technologies and in the consistent and reliable manufacture of devices in those technologies. They do not in general need to understand the final application in any greater depth than, for example, the need for approved production flows for military devices, or any requirement for unusual environmental requirements (e.g. high temperature operation).

It is essential for the skills of these three groups to overlap if the design is to be successful, but this overlap can be fairly small. In the case of XXX Ltd., the user poorly specified the device to the distributor's design team. The design team was inexperienced in the particular technology chosen, and the semiconductor manufacturer, misunderstanding the requirements of the device, proposed an inappropriate technology on the grounds of low cost. It is useful to note that once an experienced ASIC designer was brought on board the major problems were easily identified as the design system interfaces, some minor design problems, and the testing procedure. A route to a successful product was swiftly identified. None of these problems required a specific in-depth analysis of any area, merely the ability to apply normal development control processes to a new technology.

The sixth iteration of the chip was successful, and entered volume manufacture. However, due to its late arrival in the market, the product is unlikely to reach its predicted volume of sales. In the longer term, the distributor closed its ASIC design facility and formed a link to a third party design house.

6.4 Independent design consultancies.

The last ten years have seen a rapid growth in the number and size of independent design consultancies in the UK. In relation to the UK ASIC market they fall into two groups. Consultancies falling into the first group exist purely to service the semiconductor market and perform solely ASIC and standard microelectronic product design. Companies such as Phoenix VLSI, Silicon Microsystems International and Swindon Silicon Systems fall into this category. Members of the second group perform complete electronic system design, of which ASIC design forms a part. Plextek, Symbionics and The Technology Partnership are examples of such companies.

The advantage that these companies have over distributors is that they are clearly focused on design. That is, after all, where they make their money. Investment in these companies is in design related equipment, and their staff are recruited with the necessary technical and systems knowledge to perform ASIC design. Economies of scale also allow such companies to perform designs quickly and cheaply as their staff can be kept fully utilised in designing for a number of clients. Increasingly, UK and overseas companies are using such external resources rather than building internal teams.

Examples of successful products developed using this route include the TRACKER system discussed earlier, and more recently, the Ionica radio telecommunications system which was developed by a number of consultancies in collaboration with each other. These developments are discussed in some depth in the case studies section of *Chapter 3*.

6.4.1 Value chain analysis of distribution and design consultancies.

In comparing the approaches to design adopted by distributors and design consultancies, it is useful to consider the value chains of the two types of design organisations (Porter, 1985).

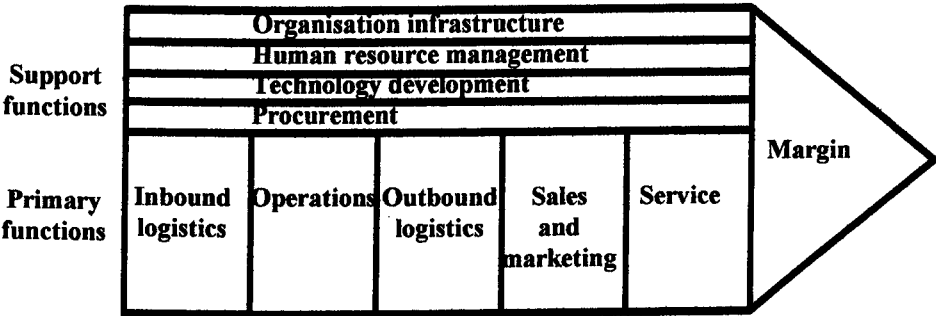


Figure 6-4. Value chain.

The value chain (*Figure 6-4*) can be used to visualise the areas in which a company adds value in producing its products. These areas can be split into primary functions (i.e. those functions which directly add value) and support functions (i.e. those functions which are necessary to support the primary functions). Clearly, different types of company emphasise, and so add greater value in, different areas to others. Consider the value chains of the two types of organisations under discussion. The areas emphasised by each type of organisation are shaded in *Figure 6-5*.

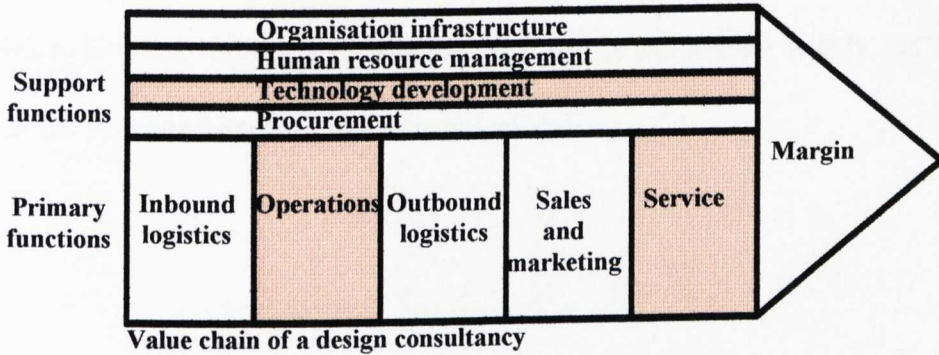
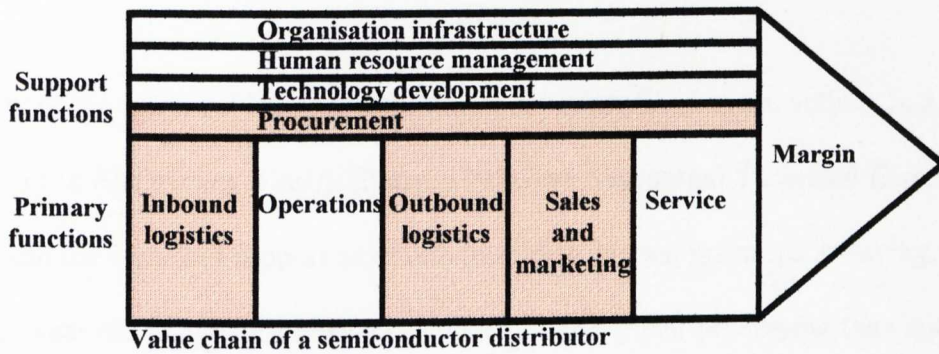


Figure 6-5. Value chains of distributors and design consultancies.

The semiconductor distributor has a value chain optimised for the sale and supply of large volumes of product. Particular emphasis is given to delivery logistics and the sales and marketing function. The whole infrastructure of such companies is optimised to reduce the cost of core functions by employing people of the lowest possible technical ability consistent with being able to take sales orders.

Design consultancies on the other hand have a single product; the service of producing high-quality designs. Their ability to survive depends on their success in producing high quality designs in a cost-effective manner. This generally leads to the recruitment of experienced design staff, investment in equipment and training, and the development of the control systems necessary to manage efficient, accurate product designs.

This view of the technical level of distribution is not confined to the author. In a report on this subject in *Electronics Weekly* (Parry, 1995) one disgruntled Technical Director, when asked about the technical support available from distributors, is quoted as saying, 'Frankly, my seven year old daughter knows more about digital signal processing than some of the jokers we have come across'. The view is supported by the Director of Engineering of the computer manufacturer Tadpole. The report concludes that many UK distributors, when faced with a technical question, can claim to do little other than supply the telephone number of the semiconductor suppliers technical staff.

6.4.2 The structure and history of the independent design industry.

According to Michael Hobday (Hobday, 1991) the independent IC design sector has its roots in the mid 1980s. He claims that in 1985 it was estimated that 45 of the 236 ASIC design centres operating in the USA were independent of semiconductor or IT systems manufacturers. The same paper claims that approximately 27 independent design centers were operating in Europe by 1986.

A survey performed by the Semiconductor Businesses Association in 1996 (SBA, 1996) established that the number of design companies had grown significantly since Hobday's survey. The SBA survey identified over 90 UK based design companies claiming to operate in microelectronic design, with a further 120 in mainland Europe. Over 80% of responding companies claimed to be independent of any particular semiconductor vendor.

Of the UK companies, 39% were less than five years old, and 71% less than 10 years old. Turnover of the companies varied, with an average turnover of around £2Million in a range of £30,000 to £14Million. The majority of design companies could claim to be SMEs according to the definitions given in *Chapter 3*. This clearly identifies a young and fast growing industry.

The design companies surveyed expressed a number of interesting attitudes regarding the skills of their SME clients when compared with those of their larger clients. These views are summarised in *Figure 6-6*.



Figure 6-6. Abilities of SME clients

It can be seen from *Figure 6-6* that in some notable areas, small clients are not seen as significantly different in skill levels to larger companies. However, there are some areas of difference. Probably the most important difference is in the lack of development capital evident in SMEs. This can lead to long selling cycles ending in the cancellation of a proposed project due to lack of funding. Small companies are also seen to be less realistic about the cost of product developments, and behind larger companies in their use of structured design methods.

On the more positive side, small companies are seen as less resistant to change, and more open to the suggestion of new technologies than their larger counterparts. In essence, this

bodes well for the adoption of ASICs by these companies. The general view of the companies surveyed regarding the UK SME user-base was that although it is not as advanced in its use of microelectronics as it might be, it consists of flexible, innovative companies who would be prepared to adopt microelectronics if the benefits could be clearly explained to them in relation to their own product needs.

Hobday (Hobday, 1991) compares the growth of independent ASIC design companies with the growth of software design companies, and indeed there are some similarities. It was when the major IT companies allowed externally produced software to be run on their machines (notably IBM in 1969), that a sector of small companies evolved, performing tasks traditionally performed by the IT company. Many such companies thrived under these circumstances; Microsoft to name but one. This can be seen as similar to the large semiconductor manufacturers releasing design information to enable third parties to design ASICs that could be manufactured using their processes.

However, there are some significant differences between the development of third-party software design and third party ASIC design. Software is generally a business tool for a manufacturing company rather than part of its final product. ASICs are clearly different in this respect. The development of ASIC technologies, and the removal of cost entry-barriers that low-cost CAE has brought has enabled an independent design industry to evolve, but the view that companies have of involving third parties in their most guarded area (new product design) is significantly different to their views on say, a new accounts package.

This structure of small, young innovative companies is typical of industries emerging to exploit a new technology. Traditionally, such an early flush of small enthusiastic

companies would quickly reduce in number as early profits due to differentiation give way to the price competition of more mature markets. This has to some extent already occurred in the independent design sector. The period from 1995-96 saw a number of mergers, takeovers and company closures. Examples include the purchase of Mosaic Microsystems by Analog Devices, the purchase of Systolic and 3soft by Mentor Graphics, the purchase of Basics by Semefab, and the demise of such companies as Array Consultants and ASIC Advantage.

One suggested role for the independent design houses is in the introduction of ASIC technology to the small or inexperienced user (Hobday, 1991) and to some extent this does occur. However, it is incorrect to assume that this role lies easily with the independent design sector. The main reason for this is discussed below.

6.4.3 High cost of 'new-name' SME business

One frequent explanation from the supply industry for their reluctance to market directly to the majority of SME companies is the expense of such marketing compared to its reward. A major concern with ASIC marketing is that the selling process is a long and highly technical one, even if dealing with potential customers who are aware of the basic principals of the technology. The buyers are engineering staff, often at a senior level, who expect to discuss their proposed application in some depth with technically competent sales staff before committing themselves. The high cost of such sales should not be underestimated. The lack of success of distributors in selling ASICs supports this.

A generalised view of the selling process for a new-name SME client is shown in *Figure 6-7*. Typical figures for the drop-out of prospective clients at each stage are shown in the diagram (McArdle, 1996:3).

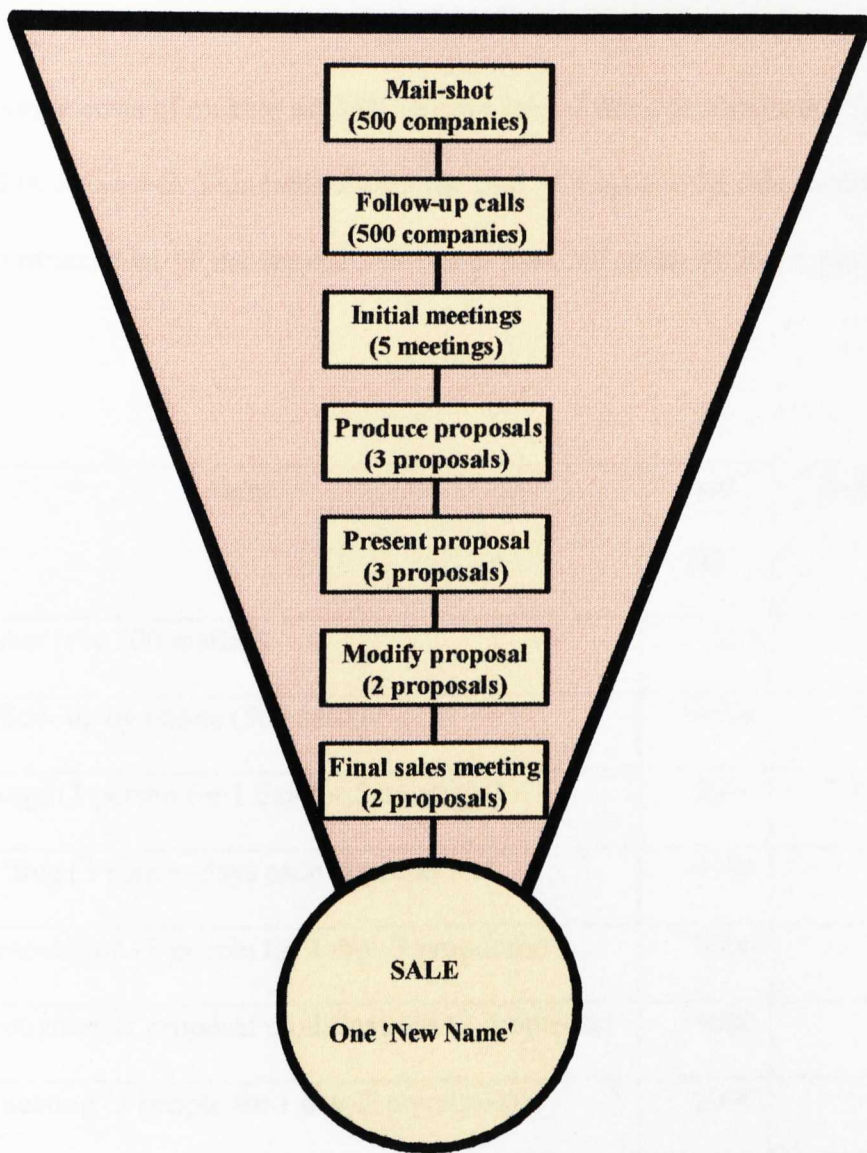


Figure 6-7. The selling triangle.

The process begins with a targeted mail-out to a large number of potential clients who must each later be contacted by telephone so as to produce a relatively small number of initial meetings. A calls-to-meetings ratio of 100:1 is not uncommon either in the experience of the author, or of professional mailing companies such as Morgan-Grampian (Anon, 1994). The initial meetings should result in the client inviting the supplier to prepare a proposal. Proposals are often modified as additional specifications emerge and final negotiations follow which eventually end in sales. This process is an involved one which can often take in excess of a year to come to fruition.

The approximate costs of making an ASIC design sale of the type shown in *Figure 6-7* are summarised in *Table 6-2*. This table shows the cost of a successful sale, which must also bear the amortised cost of the unsuccessful ones that fell away during a particular sales period.

Item	Cost (£)	Notes
Initial mailshot (say 500 mailed)	625	
Mailshot follow-up by phone (500 calls)	10500	2
Initial meetings (1 person for 1 day for 5 meetings)	2500	1
Proposal writing (3 person-days each, 3 proposals)	4500	
Proposal presentation (2 people for 1 day, 3 proposals)	3000	
Follow-up activities & proposal modifications (2 proposals)	1000	
Final sales meeting (2 people for 1 day, 2 proposals)	2000	
Expenses (travel, entertaining, subsistence)	500	
Total	24625	

Table 6-2. Cost of a 'new-name' sale

Notes.

1. Staff costs are assumed at £500 per man day. This is an average figure that a designer could be charging if doing fee earning work in place of selling. The senior staff involved in the sales process are generally even more expensive than this.

2. Assumes 25 calls per day (fairly conservative) and a telecom charge of £1 per call

So the cost of selling what might be a fairly small initial design job to an SME client is probably in excess of £20,000. It may well be in excess of this if the client requires additional visits to discuss the project, as is often the case, particularly with reluctant technology adopters.

This compares badly with the effort involved in selling to an informed buyer from a large company, particularly in the early stages because the size of the target is much smaller. In addition, while the SME may well only produce new products on an infrequent basis, the large company will often place frequent repeat business with the design company. Such business is much less expensive to sell than 'new-name' business, and consequently more profitable. It must always be the aim of any company to score repeat business with its existing customer base for just these reasons.

For these reasons, given a restricted marketing budget, an ASIC design or supply company will start by addressing the large, easily identified companies, and will only move towards addressing the more reluctant SME companies if they cannot sell all of their available resource in the former area. Alternatively, a lower cost, more focused strategy for identifying new-name business can be adopted. Such strategies include:-

- Niche marketing to a targeted subset of the SME market where specific competence can be demonstrated, or where penetration is low.
- Waiting for prospective SME new names to make contact themselves rather than being approached
- Targeting only obviously entrepreneurial, fast-growing companies
- Using new technologies for making initial contact (e.g. the Internet).

While each of these approaches has the advantage of being lower cost than the approach calculated in *Table 6-2*, they also have disadvantages. Waiting to be contacted does nothing to stimulate a market, and is unlikely to cause an increase in adoption in less entrepreneurial companies. Any sort of targeting requires specific research so as to identify targets, and any such research may be incorrect in its assumptions. Techniques such as Internet marketing are still in their infancy, and remain unproven.

The conclusion from this cost model is that potential SME users are unlikely to be encouraged by suppliers and in consequence are more likely than large companies to be badly informed about ASIC technology. This is a major reason why government intervention can be useful in encouraging technology adoption.

If a government believes that technology adoption is beneficial to the industrial base, they can effectively perform the early marketing activities (awareness, information, training, encouragement) and then present the supply industry with pre-qualified sales leads. In essence, this is the approach that has been adopted by the main government initiatives discussed in *Chapter 9*.

It would then seem that marketing to SME users is not economically viable if the only source of revenue for the design-house is that generated in the design. This has led a number of design companies to adopt a different strategy with their SME clients. That strategy is to offer both a design service, and subsequently a supply service. This is discussed in more detail in the next section.

6.4.4 Beyond third party design - Design and supply.

In discussions with potential users of ASIC technology in association with the MiB programme, an important facet of the market became evident. There seemed to exist a significant number of potentially large-volume ASIC users who were using alternative technologies (e.g. electromechanics, hydraulics) because they had no concept of where to start to incorporate electronics, let alone ASICs, into their products. These companies were faced with a step that seemed so huge (new design techniques, new design tools, new design staff, new production techniques, new suppliers, new inter-company relationships, new logistics, new marketing techniques, new markets) that they were simply unable to make the change. For many such companies it would have been foolhardy to attempt such a massive step. In order to meet the needs of this market it is necessary to attempt to supply a complete solution. The requirement is not only for the design and supply of ASICs, but of complete application specific electronic units.

For example, washing machine manufacturers may not want to design or even purchase ASICs to go into an electronic controller. They may want to buy complete designed, built and tested controllers. Some small companies do exist to service these 'design and supply' needs in specific niche markets, but in 1995, most of these companies operating in the UK were using outdated technology, and few if any were able to perform ASIC design. There were also a number of sub-contract assembly companies who could build electronic sub-assemblies once they had been designed, but had no advanced design facilities. There was clearly a market need to provide cost effective, high-technology design and supply in high volumes to a number of users.

These market needs have been met by the emergence of a number of product supply companies from the design-houses. Some are supplying ASIC devices to the more sophisticated user (e.g. Swindon Silicon Systems) while others have gone as far as forming joint-venture companies with high-volume electronic manufacturing companies so as to be able to supply complete electronic sub-assemblies (e.g. the Unico Communications alliance between Plextek and Unico Technology).

By using this strategy, these companies have been able to offset the high costs of initial marketing not only through sales related to the design process, but subsequently through sales of finished products.

6.5 Conclusions on the UK ASIC supply industry and its customers

The analysis of the industry and its customers performed in this chapter leads to a number of conclusions of particular relevance to the adoption of ASICs by UK industry.

The first major conclusion is that there is no single 'market' involved, but a wide range of market segments that often have little in common other than the possibility of using electronics in their products. Within each of these segments, users may be at a different stage in the adoption process. This presents a very difficult marketing problem.

There is a young and volatile design and supply industry serving these markets. This industry is undergoing constant radical change, and is likely to continue to do so for the foreseeable future.

The economics of marketing suggest that companies offering design services are unlikely to market to SME clients, preferring to concentrate on the more lucrative clients in larger companies. However, for SME users with higher product volumes, 'design and supply' companies might offer an alternative.

7. Reasons for non-adoption given by potential users.

Previous chapters have shown that ASICs can bring competitive advantage to SMEs and that a design and supply industry exists that is capable of meeting their needs. Some barriers to successful marketing have been identified, but it remains that UK companies are failing to take advantage of a technology that could bring them considerable rewards.

In this context, it is important to analyse the views of the potential ASIC users regarding the use of microelectronics in their products and to analyse the reasons that they give for not taking advantage of the technology.

This chapter aims to identify the reasons given by potential users for not adopting ASIC technology, and to investigate whether those perceptions are based in fact.

7.1 Methods of investigation.

To investigate the reasons why companies do not adopt ASIC technology, a number of methods were employed including:-

- A questionnaire to companies who do or might use microelectronics in their products
- Discussions with potential and current users
- A literature search
- Discussions within the design industry's trade associations

7.1.1 Questionnaire.

A questionnaire was mailed to potential and current users of microelectronic technology. The majority of those questioned were delegates of the DTI Microelectronics in Business seminars, but a set of non-attendees was also surveyed to check that MiB attendees did not represent a skewed sample. The reason for using the former group was mainly because other questionnaires had indicated some very anomalous results, perhaps suggesting that those questioned did not fully understand the questions. After attending one of the MiB seminars, people might at least be expected to understand more of the terminology used in the questionnaire than those with no prior knowledge.

The questionnaire was piloted in 1994, some modifications made, and the main survey performed during the remainder of the research period so that possible trends could be investigated. The format of the questionnaire is shown in *Appendix B*. Its basic design follows the guidelines discussed in *Chapter 5*.

7.1.2 Discussions with users.

During 1994, 1995 and 1996, the author was a presenter of the two series of management seminars that formed part of the DTI 'Microelectronics in Business' initiative. This initiative is discussed in detail later, but presented the author with the opportunity to discuss in detail the reasons and trends identified in the questionnaire with several hundred seminar delegates. Also, in over 30 seminars, the same questions were asked by delegates time and time again, giving additional indications of major concerns. In addition, the author's work as a design consultant brought him into contact with a wide variety of electronic equipment companies with whom discussions were held to develop ideas relating to the reasons identified from other sources (e.g. the user survey).

7.1.3 Literature search.

The most relevant previous research published regarding reasons for non-adoption of ASICs was that of by Michael Shortland Associates in the late 80s (Shortland, 1991). This study is discussed at length in *Chapter 4*, but it seems that perceptions have changed little between the time of that survey and the one performed for this study. Shortland found that the main reasons given for non-adoption were:-

- Cost of entry
- Lack of a second source
- Lack of skilled designers
- Risk of failure

7.1.4 Discussions with Trade-Associations.

The two UK trade associations most active in the area of this study are The Semiconductor Businesses Association (SBA) and the Federation of the Electronics Industry (FEI). Both of these organisations made a significant contribution to the discussions involved in the construction of the DTI's Microelectronics in Business programme, and this study draws on some of the discussions held in association with that activity and some subsequent correspondence with the FEI (Whittaker, 1994)

7.2 Questionnaire results.

The user-questionnaire described earlier contained a number of questions regarding the reasons that respondents had for not adopting ASIC technology. These were contained in section 8 of the questionnaire as a series of Likert scales.

A summary of the responses given by users in that section is presented in *Table 7-1*.

	Statement.	Percentage agreeing
1	ASICs can increase our products unique features.	79%
2	Small companies don't do ASICs.	26%
3	If we wanted to use ASICs We'd know where to go.	56%
4	ASIC suppliers ignore our company.	44%
5	ASICs can lower our products raw materials costs.	62%
6	Only large companies have engineers capable of ASIC design.	24%
7	ASICs cost less to design than alternative technologies.	15%
8	The risks involved in using ASICs are higher than with other technologies.	50%
9	ASICs can lower our manufacturing costs.	62%
10	NRE charges for ASICs are too high for us to use them.	56%
11	ASICs can lower our test costs.	56%
12	ASICs take too long to design & prototype.	53%
13	ASICs can reduce the size of our product.	76%
14	The cost of entry to ASIC use is high compared to other technologies.	79%
15	If we don't use ASICs our products will be left behind.	44%
16	Our volumes are too low to justify the use of ASICs.	56%
17	Our designers have no experience of ASIC design.	82%
18	My competitors are using ASICs.	41%
19	Small companies are fully capable of ASIC designs.	79%
20	Many successful ASIC designs come from small companies.	85%
21	The DTI promotes the use of ASICs in a positive way.	94%
22	The DTI 'Microelectronics in Business' initiative will increase the uptake of ASICs in the UK by smaller companies.	88%
23	We cant predict the sales volume of our product in advance, so don't know if ASICs are justified.	35%

Table 7-1 Attitude question responses.

These results are summarised graphically in *Figure 7-1*.

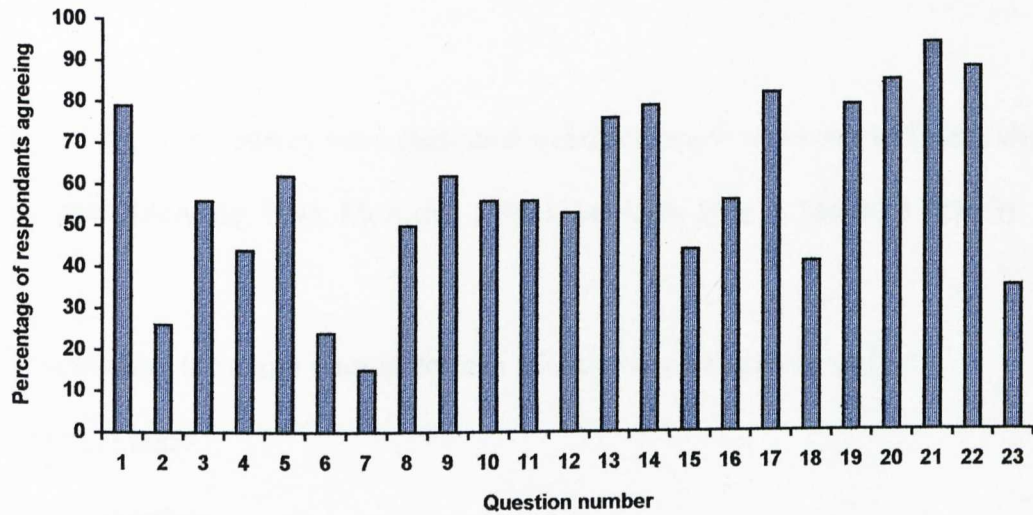


Figure 7-1 *Attitude question responses*

Clearly, cost is still the major issue, with most respondents (79%) feeling that entry costs are higher than comparable technologies and that ASICs cost more to design than other technologies (85%). A number of responses suggest that people believe that small companies are fully capable of ASIC design, but only 18% of respondents feel that their own engineers have experience of the technology. The proportion of companies believing that economic volumes are a problem (56%) is less than Shortland found, but nonetheless still significant.

Companies are coming around to the idea that ASICs could do some good for their products, believing that they could add unique features (79%), reduce raw materials costs (62%), reduce manufacturing costs (62%), and reduce product size (76%).

There also seems to be a high level of support for government intervention with 88% of respondents believing that the DTI technology transfer scheme (MiB) would increase technology adoption.

The results of this survey were published and discussed in a number of papers during 1995 and 1996 (McArdle, 1995. McArdle, 1996:1. McArdle 1996:2. McArdle 1996:3).

In conclusion, the major reasons for non adoption can be summarised as:-

- Cost of entry.
- Risk of failure.
- Single sourcing.
- Lack of trained staff.
- Insufficient production volumes.

These major concerns are believed by the author to be incorrect perceptions rather than real reasons. In order to investigate this, each of these reasons is now investigated. The remainder of this chapter takes these perceived reasons one-by-one and investigates whether they are based in fact.

7.3 Cost of entry.

Cost of entry is repeatedly given as the primary reason for non-adoption by potential ASIC users. If it can be demonstrated that this is an incorrect perception rather than a fact, we can go some way towards eliminating a major hurdle to ASIC adoption.

7.3.1 ASIC design flow

Each of the ASIC technologies discussed goes through a similar design route. However, the emphasis on each stage may vary according to the technology being used. The outline design process is shown in *Figure 7-2*. It is important to understand this process, as many of the cost and risk implications of the use of these technologies stem from it.

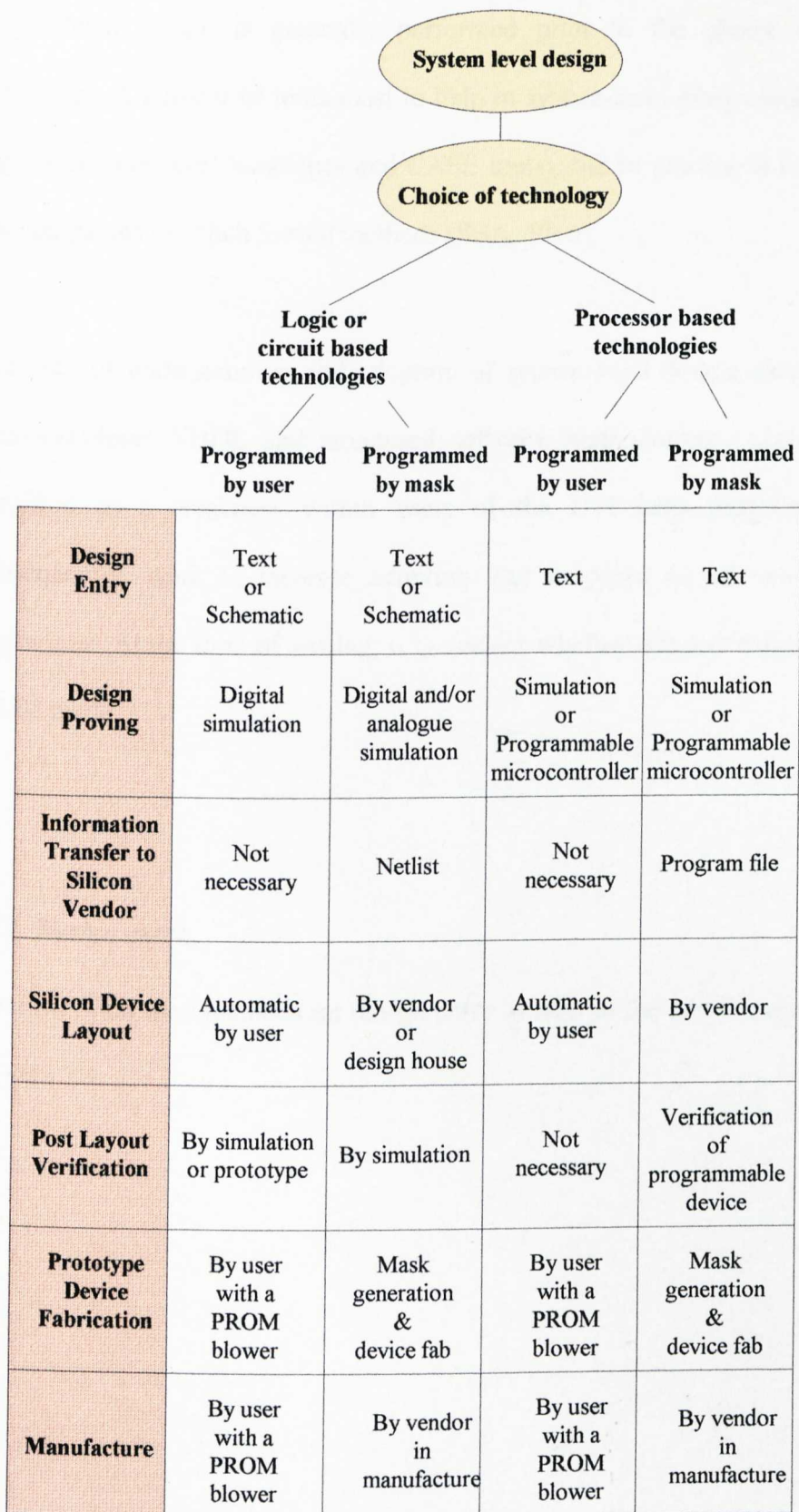


Figure 7-2. ASIC design flow

System-level design is generally performed prior to the choice of implementation technology. A number of tools exist to help in system-level design and technology choice (e.g. behavioral level languages and CASE tools), but in practice it has been shown that few companies use such formal methods (SBA, 1996).

This lack of understanding and adoption of system-level design methodologies such as behavioral-level VHDL and structured software methodologies such as Yourdon was identified as a weakness within users of the DTI MiB programme during 1996. Consequently, work to increase adoption was proposed as an extension to the MiB programme. At the time of writing, it is unclear whether this extension to the programme will be made.

7.3.2 *Design entry.*

The most often used methods for design entry in each of the ASIC technologies are shown in *Table 7-2*.

Technology	Design Entry Method.
Programmable Logic Devices	Text Entry & Synthesis or Schematic Capture
Microcontrollers (masked and user-programmable)	High & Low Level Programming Languages
Gate Array (all digital)	Text Entry (HDLs) & Synthesis or Schematic Capture
Cell Based Devices (digital, analogue and mixed-signal)	Text Entry (HDLs) & Synthesis or Schematic Capture

Table 7-2. Design entry methods

Microcontrollers stand alone because, being software driven, the tools available for programming them are software development tools. The sophistication of the tools varies with the family of microcontrollers chosen. It ranges from simple assemblers for the microcontroller's native code (e.g. 8051 machine code), to high-level language compilers for a range of high-level languages (e.g. C).

All of the other devices, being hardware devices by nature, are designed using techniques which have become normal for contemporary hardware engineers. The sophistication of these tools varies from schematic capture, where the designers use a drawing package to draw a circuit diagram using the basic building blocks available to them (e.g. gates, latches) through simple textual entry and synthesis tools such as PALASM, through to complex behavioral languages which can be used to describe functions at a high level of abstraction. These descriptions are then used in conjunction with sophisticated hardware

synthesis tools to produce gate-level implementations of the design. However, current implementations of synthesis tools will require an intermediate level of abstraction such as register transfer level (RTL) VHDL to be derived from the abstract behaviour as they are not yet capable of translating behavioral descriptions directly into gates. The relative merits and basic costs of these tools are summarised in *Table 7-3*. The costs relate to the cost of the software tools rather than to those of the platforms on which the tools run.

Type of software tool	Example	Features	Platform	Cost of software tool
Assembler	Keil 51	Low level language translation	PC	£300
Schematic Capture	ORCAD	Simple schematic capture	PC	£200
	Intergraph AcePlus	Complex schematic capture	Workstation	£5000
Hardware Description Languages	VHDL, Verilog	High level of abstraction. Complete system modeling	Workstation (some lower cost PC versions are available)	£15000
Hardware Synthesis	PALASM, ABEL	Simple synthesis aimed at specific programmable devices	PC	£200
	Synopsys	Advanced, technology independent synthesisers	Workstation	£20,000

Table 7-3. Design entry tool costs.

It can be seen from *Figure 7-3* that low-cost systems, attractive to small and new users of ASIC technology are readily available, although the functionality of the low-end products is considerably less than that of their more expensive counterparts. For example, while a £200 design-synthesis tool such as PALASM is capable of translating Boolean equations to compile the fuse-map of a PAL it can not be used for other technologies. At the time of writing, some very low cost VHDL and synthesis tools are beginning to appear on the market. These tools are aimed at specific low-end devices and normally support only a subset of the VHDL language, but with prices as low as £79 will undoubtedly have an effect on the uptake of VHDL.

7.3.3 Design proving & simulation.

In this area, the techniques vary according to the technology, its complexity, and the risks and costs associated with incorrect designs. The major design proving tools are shown in *Table 7-4*.

Technology	Design Proving Method.
User-programmable logic devices	Simulation Emulation Trial and error
Masked and user-programmable microcontrollers	In-circuit emulators EPROM & OTP devices
Gate-arrays (all digital)	Simulation Emulation using programmable logic
Cell-based devices (digital, analogue and mixed-signal)	Simulation Emulation using programmable logic

Table 7-4. Design proving methods.

Microcontrollers are generally proven prior to final fabrication by using an in-circuit emulator. This is a device which connects to the product in the place of the microcontroller and emulates the behaviour of the microcontroller and its software, often under the control of a PC. The emulator is able to run the microcontroller code written for the application. Emulation systems have the advantage of software debugging and tracing tools to help the programmer debug the code. Another method used to check a microcontroller design is to program the target code into a low-cost programmable version of the final part. Many microcontrollers have an Erasable Programmable Read Only Memory (EPROM) version, which can be repeatedly reprogrammed, or a One Time Programmable (OTP) version which can be programmed once in the laboratory. Although considerably more expensive than a masked part (often a factor of ten times more expensive), these devices are frequently used in early production runs of products so as to

verify the correctness of the program prior to releasing program information for a masked version of the chip for use in higher-volume manufacture.

For the other devices, simulation remains the most effective method of ensuring that the devices meet their specification prior to prototype fabrication. A variety of simulation tools exist ranging from simple logical state simulators such as that found in PALASM, through complex digital timing simulators to component-level analogue simulators.

The most commonly used simulators for digital ASIC design are the digital timing simulators which combine the prediction of logical states with calculation of the timing of state transitions. Device-level analogue simulators, which are mainly based on SPICE are generally only used to characterise an ASIC family, defining its characteristics for simulators which require less processing power to operate. The less complex simulation methods can then be used by the application designer (e.g. digital models or analogue behavioral models). Indeed, the amount of computational power that would be required to simulate a large gate-array through a design proving set of test patterns at the transistor level is not practically achievable.

For masked ASICs, emulation using programmable logic is often cited as an acceptable route to design proving, with many programmable-logic vendors claiming that the migration from a programmable device to a masked ASIC is then a simple, automated translation exercise. The author disagrees with this approach for a number of reasons:-

- The size of available programmable devices means that complete ASIC designs can rarely be incorporated in a single programmable device. The resultant partitioning is

then unrepresentative of the final device. This is however becoming less of an issue as programmable devices with over 50,000 gates become commonplace.

- The basic building blocks of programmable devices are different to those used in masked technologies, often leading to an emulator design that diverges significantly from the ASIC being emulated.
- Device timings are radically different between programmable and masked technologies, causing major differences in function, even in highly synchronous designs.
- Direct translation from one family to another rarely makes optimal use of the target family's capabilities and results in unnecessarily large ASIC devices.

As a result of these differences, examples of ASIC emulation using these methods that the author has experienced have normally ended up with two divergent developments; one of the masked ASIC, and one of the programmable emulator. While this may be desirable if some form of hardware is required early in the development to prove other parts of the system, it can not be regarded as anything but a very rudimentary check of the final ASIC. Far better results can be obtained more cost effectively by using simulation.

The range and relative costs of these design proving methods are summarised in *Table 7-5* below. The costs discussed here do not include the cost of the hardware platform on which software tools run, but do include the cost of specific hardware (e.g. the in-circuit emulation hardware)

Method	Example	Features	Platform	Cost
In Circuit Emulator	NEC 17k Emulator	Hardware Emulation Software Debug Tools	PC	£600 (includes emulator hardware)
Digital Simulators	PALASM	State Only Device Specific	PC	£200
	Intergraph Advansim	Full 16 state Digital Timing Simulator. Logic Analyser Features. Extensive user interface.	Workstation	£10,000
Analogue Simulators	SPICE	Basic analogue simulation	PC	£500
	Intergraph APEX	Advanced features such as component spread	Workstation	£15,000

Table 7-5. Design proving methods - costs.

7.3.4 Information transfer to the silicon vendor.

This process does not normally take place for user-programmable devices of either the logic or processor based types. For these devices, prototype manufacture is invariably an in-house process performed on a simple device programmer (a PROM programmer). Some processes do exist to transfer the design of a programmable logic-based device to a masked equivalent (e.g. the Xilinx 'Hardwire' array) but this route is seldom taken as the resulting chip often fails to gain the advantages of a masked solution as the die-size and hence cost of the resultant part remains too close to that of the programmable part to make the engineering effort involved cost-effective.

For masked microcontrollers the program information is transferred as a file of the compiled program, often in an EPROM or on a floppy disc. There is little opportunity for error in this process, but the code delivered to the silicon vendor is normally reprogrammed into another EPROM and returned to the user for verification. Once verified there is no further interface between the silicon vendor and user until the device is produced in prototype quantities.

For masked logic or circuit-based devices, the process is more involved. The layout of the device is normally performed by the silicon vendor, although some exceptions do exist in very experienced users who prefer to perform the layout of their own devices in order to maximise performance, or in security sensitive users who do not wish to let design information leave them.

In order to perform the layout a silicon vendor requires a list of component-to-component connections (a netlist) and a set of stimuli and responses describing the behaviour of the

circuit that can be applied by production test equipment to test manufactured parts (test vectors). The layout, and its subsequent simulation using the test vectors, will often be performed on a different software system from that used for initial designs, so this stage of the process may involve a translation and transfer of the netlist and test vectors in a machine readable form understood by both systems. Tools to perform these tasks are generally integral parts of the more expensive computer aided engineering (CAE) packages. In order to check that this process has been successful, post-layout simulation is usually performed. This is discussed later in this chapter.

7.3.5 *Silicon device layout.*

The design provided by the user is taken by the silicon vendor and converted to a layout and eventually a photolithographic mask or reticle set. In the case of gate-arrays and standard-cell products (and some programmable-logic families), this layout can affect the behaviour of the circuit, as the metal interconnect introduces parasitic components (resistance, inductance, capacitance) which can change the timing and performance parameters of the circuit. These effects are checked in post-layout simulation.

It is opportune to discuss relative Non-Recurring Engineering (NRE) charges at this stage as the silicon vendors often claim that these are levied mainly to cover the costs that they incur in layout and mask tooling. Typical NRE charges for the various technologies are shown in *Table 7-6* below.

Programmable logic devices also go through a layout stage, which is performed by the user using the tools supplied by the vendor. The result is a fuse pattern to be used on a prom

blower (e.g. in a PAL), or a connectivity pattern to be downloaded to a device on initialisation (e.g. in a Xilinx FPGA)

Technology	NRE (£)	Includes
User-programmable microcontroller	zero	Program is loaded into on-chip memory
Masked microcontroller	2000 -5000	Mask for program metalisation, automatically generated.
Programmable logic device	zero	Layout is performed on vendor supplied design software
Gate array	5000 - 100,000	Engineering support. Test vector simulation. Layout. Mask set for interconnect layers.
Cell-based device	30,000 - 200,000	Engineering support. Test vector simulation. Layout. Complete mask set for all layers.

Table 7-6. ASIC NRE charges.

7.3.6 Post layout verification

For both masked and user-programmable microcontrollers, post-layout verification prior to fabrication is rarely performed. It is assumed that no errors can be introduced in the layout process.

With some types of programmable-logic devices, parasitic components of the type discussed earlier can be introduced in layout, and post-layout tools are available to simulate the behaviour of the device including the parasitic effects introduced in the layout process. However, post-layout simulation is often omitted by the user, who may prefer to fabricate a device and try it 'in-circuit' due to the low cost and short time penalties of reiteration with this type of device.

In contrast, for devices involving the production of a mask set, the cost of reiteration is relatively high. In the UK, silicon vendors generally charge about £2000 per mask, and a full mask-set may typically be as many as thirteen separate masks. Additionally, reiteration will involve considerable engineering effort in redesign and layout. Consequently a high degree of post-layout verification is generally performed to ensure that parasitic components added during circuit layout are not significantly different to those assumed by the designer before the layout was performed. This will often involve a further translation stage so that values for post-layout parameters can be transferred back to the CAE system on which the chip was initially designed.

It is not the object of this study to cover the design process in great detail, but the author's experience of investigating the reasons for failed designs on behalf of clients has shown that designs which are unsuccessful often result from a failure to close the loop between

pre-layout and post-layout simulations. Proper post-layout simulation can catch a wide range of errors from subtle timing errors introduced in layout to gross connectivity errors introduced in netlist translation or layout tools, and can often be performed using automated methods over the course of a few days following the layout of the device. ASIC designers skimp on this stage at their peril. It is important in choosing suitable vendors and tools to check that this loop can be closed. This is a relatively subtle consideration which is often overlooked by less experienced designers.

7.3.7 Prototype device fabrication.

For user-programmable devices of all types this stage is performed using a device programmer costing a few hundred pounds. For masked devices it is performed at a silicon foundry. While programmable devices can be fabricated in a few minutes, masked devices generally take 4 to 6 weeks for gate-arrays, 12 weeks for microcontrollers, and up to 16 weeks for cell-based products. However, it should be noted by potential users that the actual processing time for a complete mask-based product is only a few hours. Most of the weeks of waiting is taken up in queuing time through the various stages of the silicon foundry.

7.3.8 Comparative cost totals for the new entrant.

One of the most important questions posed by the potential new user of ASIC technologies is, 'What will it cost?'. A summary of typical hardware, software & NRE charges that might be expected by a new user wishing to do his own designs is shown in *Table 7-7* below. The costs are those which would result in a small number of prototype devices.

The gate-array and cell-based costings are based on a 10,000 gate digital design which although considerably below the 40,000 gate average for current designs might well be the sort of size that a new SME user might try as a first design. It should be stressed that these are typical list prices. Methods of reducing these costs are discussed later in this chapter.

	Programmable microcontroller	Masked microcontroller	Programmable logic device	Gate array	Cell-based device
Hardware					
PC System	2,000	2,000	2,000		
Workstation				10,000	10,000
Software					
CAE software for design entry & simulation	200	200	500	20,000	20,000
Emulation	600	600			
NRE charges		3,000		30,000	70,000
Prototype devices	100		100		
PROM blower	500		500		
TOTAL	£3,400	£5,800	£3,100	£60,000	£100,000

Table 7-7. Typical direct entry costs for ASIC technologies.

Indirect costs.

The only costs involved in the introduction of ASIC technology which are not covered in *Figure 7-7* are the less tangible, indirect costs. The most significant of these are those concerned with people. They are:

- Recruitment of experienced ASIC designers
- Training of existing staff in ASIC technology
- Continued training as new technologies emerge

All of these areas may represent major investments for a new user of ASIC technology, but it is unlikely that a user would expect to recover such investment in the development of an individual product. Training and recruitment are strategic investments and need to be considered as part of the overall strategic plan of the company (Ivey, 1994). If that plan includes the use of microelectronic technology to achieve competitive advantage, then these costs must be met. The level of such costs can range from quite low (e.g. for training an existing engineer in the use of programmable technologies) to relatively high (e.g. recruiting and maintaining a team of masked ASIC designers).

7.3.9 *Methods for reducing cost of entry.*

The figures given above should be regarded as typical rather than minimum, and a number of commercial and technical approaches exist which can be used to reduce or eliminate the costs shown in *Figure 7-7*.

Reducing cost of entry for masked and user-programmable microcontrollers.

It is possible that the sort of PC system necessary to run the software development tools needed to develop code for a microcontroller already exists in the company, so negating the need to buy one. In addition, design-entry software and emulators may be rented at low cost or even borrowed free of charge from a distributor or manufacturer who feels that the design might result in the purchase of large volumes of the microcontroller chips. When a masked microcontroller is used, the user also has the option of using EPROM or OTP versions of the device in early production runs so as to defer the point at which the NRE charge needs to be spent to produce a lower-cost part in higher volume.

Reducing cost of entry for programmable logic devices.

The entry-costs for programmable logic devices can be reduced in much the same way as those of microcontrollers. Existing PC hardware can be used to run the design tools, and the tools themselves can often be loaned free of charge or hired from device manufacturers and distributors. This approach was taken by Wicks and Wilson Ltd. (Ivey, 1994). They designed and manufactured a microfilm enhancement tool using Actel FPGAs and were able to hire the development system for £300 per month until they decided that the technology was an appropriate one.

Reducing the entry cost of mask programmed devices.

A number of methods also exist which will allow the £60,000-100,000 quoted earlier to be reduced. The CAE hardware and software discussed is generic software capable of designing ASICs for fabrication by a number of manufacturers. If the user is designing

small ASICs (i.e. a few thousand gates) then simple PC based tools may be sufficient. Alternatively, if the user is prepared to tie himself in to a single manufacturer then that manufacturer might be willing to provide tools specific to their products at a lower cost or even on a free loan.

NRE charges can also be reduced by a number of methods. The first method is to negotiate with the manufacturer to amortise the charges over the first few thousand production devices. In this way a £30,000 NRE might become an additional £30 on each of the first 1000 production chips. However, in order to do this a manufacturer will generally require a minimum order for the necessary number of production parts to be placed before prototypes are delivered. This is simply a way of postponing the payment, rather than eliminating it, and the total financial risk is increased as a minimum number of production chips will now have to be bought irrespective of the success of the product.

Another method of reducing NRE charges is by participation in multi-project wafer (MPW) developments. In this case the area of a prototype wafer is split between a number of designs. In this way some of the prototype costs can be split among participants. This can significantly reduce NRE charges. For example, in an interview in *Electronics Weekly* (Anon, 1995:3) Thesys Microelectronics claimed NRE charges as low as £2,300 including the delivery of 5 prototype parts. This method is often used by academic institutions, or commercial organisations where production volumes are known to be low, or the development known to have a high technical risk. It has a number of disadvantages including having to wait for all of the other designs being fabricated on the wafer to finish before prototypes can be made, and the problems of having either to re-engineer the mask-set or waste significant amounts of silicon area (other people's chips) if higher volumes

require additional wafers to be manufactured. Proponents of this approach operating in the UK include Micro Circuit Engineering (MCE) and Austria Micro Systeme (AMS). An MPW service is also available as a Europractice basic service. This European initiative is discussed in greater detail later in *Chapter 9*.

The use of such MPW services is common throughout the rest of the world, and some of the services available are detailed in *Table 7-8*. The table details those providers working mainly with industrial rather than academic users. (Courtois, 1995).

Country	Provider	Services
Australia	Joint Micro-electronic research centre (JMRC)	Active in 80's, now believed extinct.
Belgium	IMEC/INVOMECE	Mietec CMOS Became part of Eurochip
Brazil	Project Multi User (PMU)	VTI CMOS ES2 CMOS SiD-Microelectronica bipolar
Canada	Canadian Microelectronics Corporation (CMC)	NT CMOS Gennum Corp Bipolar Mitel CMOS (micromachines)
France	CMP	ES2 - CMOS SGS-Thomson - CMOS
Germany	Fraunhofer Institute for Integrated Circuits (FhG-IIS)	AMS - CMOS ES2 - CMOS Mietec-Alcatel BiCMOS
India	Government Department of Electronics (DOE)	None yet
Ireland	National microelectronic research centre (NMRC)	In-house CMOS
Italy	Microelectronics development association (MIDA)	ES2 - CMOS AMS - CMOS LSI LOGIC - CMOS
Japan	Advanced software technology and mechatronics research institute (ASTEM)	ES2 - CMOS FED (under development)
Korea	Inter-university semiconductor research centre (ISRC)	Orbit - CMOS
Malaysia	Malaysian institute of microelectronic systems (MIMOS)	NORCHIP - CMOS (see below)
Scandinavia	Norchip	AMS - CMOS
Switzerland	Swiss federal institute of technology (EPFL)	SGS-Thomson - CMOS ASCOM - Bipolar
Republic of China	Chip implementation centre (CIC)	CMOS

Table 7-8. Multi-project wafer services worldwide.

Reducing all direct and indirect costs.

For some companies, addressing the direct and indirect costs discussed in this chapter by recruiting and equipping an ASIC design team does not represent the best business model for their organisation. Many large and small companies prefer to use the services of an external design-house to perform the technology-specific parts of the design process while

concentrating their internal skills at the system level. Ionica, TRACKER, and Waterside, discussed in *Chapter 3* are all examples of companies who adopted this approach. The use of third-party design and the growth of the 'network company' was discussed in some detail in *Chapters 3 and 6*.

7.3.10 Conclusions on cost of entry.

Given the analysis presented in this chapter, it can be shown that cost of entry to the use of ASIC technology can be very low. For some technologies it is virtually zero, and in most cases it is lower than the costs that many companies routinely face (for example in the purchase of a company car). The fact that potential users perceive high costs to be associated with the adoption of ASIC technology must be considered as a real problem, but the actual cost should not be a barrier to even the smallest companies.

7.4 Lack of skilled designers.

Lack of skilled engineers is another major reason cited by potential ASIC users as a reason for non-adoption. According to DTI figures, the UK has approximately 27,000 electronic design engineers, excluding managers, with over 7,500 working for SMEs. It is possible that many of these engineers (particularly the younger ones) will have encountered ASIC technology during undergraduate or postgraduate education. However, their senior managers do not consider them sufficiently skilled to use ASIC technology.

It is a hypothesis of this study that the skills necessary to adopt ASIC technology include not only technical, but business and commercial skills, so it was necessary to investigate the extent of these skills in UK industry, and the validity of the senior managers perception that such skills do not exist within their organisations.

7.4.1 Method of investigation.

In order to ascertain the level of training in ASIC design available within companies electronic design departments, and the level of ASIC specific education in UK universities, a survey of the heads of department of all UK universities with an electronics department listed in The Commonwealth Universities Yearbook (Association of Commonwealth Universities, 1994) was performed. A total of 49 institutions were included in the survey. The layout of the questionnaire, which can be seen in *Appendix C*, follows the design rules for questionnaires discussed in *Chapter 6*, and was intended to ascertain the level of education in technical, business and commercial skills related to ASIC technology that was being included in undergraduate and postgraduate courses.

After 4 weeks, 20 questionnaires had been returned. A reminder was sent to non-respondents. This resulted in a total of 25 responses. The results are summarised below

7.4.2 Results of the university survey.

The first section of the questionnaire aimed to ascertain the level of technical education relevant to ASIC design that is available to first and higher-degree students. The questionnaire asked whether particular skills were included in the degree course. The number of institutions answering 'yes' to particular skills is summarised in *Table 7-9* below.

Skill	First Degree	Higher degree
PLD design	89%	42%
FPGA design	68%	37%
Masked gate array design	47%	16%
Standard cell IC design	42%	26%
Full custom IC design	37%	26%
Schematic capture	89%	42%
HDL design entry (e.g. VHDL)	42%	26%
Logic synthesis	47%	42%
Design for test (e.g. scan path)	63%	26%
IC layout techniques & tools	53%	47%
Digital simulation	95%	47%
Analogue simulation	95%	47%
Behavioral simulation	37%	32%
Analogue IC design	32%	26%

Table 7-9. University responses regarding technical skills.

Clearly, most universities have a significant amount of material on ASIC related technical skills included in both undergraduate and postgraduate courses. It would follow that graduates should at least be able to begin to tackle the technical aspects of an ASIC design.

Business skills also figure significantly in the content of degrees, as can be seen from *Table 7-10*.

Skill	First Degree	Higher degree
Break-even analysis	42%	11%
Net present value analysis	26%	5%
Presentation skills	84%	21%
Project planning (e.g. Pert, Gannt)	89%	26%
Critical path analysis	79%	26%
Product lifecycle planning	53%	11%

Table 7-10. University responses regarding business skills.

The inclusion of business skills in university courses is partly due to the efforts of the Institution of Electrical Engineers. Degree syllabuses need to be approved by the IEE if the qualification is to exempt the graduate from examinations for corporate membership, and although chartered status is not held to be as valuable in electronic engineering as it is in say mechanical or civil engineering, most courses aim to be approved, and most students would think twice before joining a course which is not.

However, when asked questions on purely commercial rather than business topics, the response is not as positive. Few universities produce graduates who could answer even basic commercial questions about the technologies which they have been taught to use. In the third section of the questionnaire, institutions were asked whether their graduates would be able to correctly answer certain commercial questions. The percentage responding 'yes' to particular questions is summarised in *Table 7-11* below.

Question	First Degree	Higher degree
Can you name 3 manufacturers of FPGA	32%	37%
Can you name 3 manufacturers of masked gate-arrays	16%	26%
Can you name 2 manufacturers of mixed-signal standard-cell ICs	21%	26%
What is the likely NRE charge for a 50,000 gate gate-array	21%	11%
What is the likely part cost for the above gate-array in 10K quantities	16%	11%
What is the part cost of a 2000 gate FPGA in 100 off volumes	26%	16%
What is the cost of a 4 bit microcontroller in 100K quantities	16%	5%

Table 7-11. University responses regarding commercial skills.

There seems to be a wide range of opinion on the inclusion of business and commercial skills in degree courses, with this section of the questionnaire generating the highest number of additional comments.

One university (Manchester Metropolitan) clearly think commercial skills important and have their students consider a product development for which they calculate the cost of

using two alternative technologies (masked ASIC and microcontroller). The cost of both development and production are considered. In contrast, another university (Bristol) responded by commenting, “ Why do students need to know these things - surely they just pick up a telephone to find out. These questions are pointless”. As the same respondent replied that their students would not be able to name three manufacturers of gate-arrays, or two of standard-cell, it is unlikely that they would be able to ascertain this price information without further training.

7.4.3 The role of the IEE in shaping graduate skills

In discussions with the academic community it became clear that even those resistant to introducing, ‘ephemeral’ topics such as the costs of the various technologies felt that they were being forced to include such topics in order to qualify as an accredited course with the Institution of Electrical Engineers. This subject was raised in correspondence with the IEE. The influence of the IEE on the training of engineering graduates is summarised in their ‘Guidelines on Accreditation’ (IEE, 1991:1).

Since 1979 the IEE has used its accreditation scheme to approve specific degree courses and exempt graduates of them from the institution’s entrance examinations (IEE, 1991:2). Accreditation reviews are performed by panels which are made up of academic and industrial members who as far as practicable follow the structure established by the Finiston Report, ‘Engineering our future’ (Finniston, 1980). The report calls for a four-phase approach to engineering training (EA1 - EA4). The basic structure of each of the four phases shown in *Figure 7-12*.

Phase	Structure
EA1	An introduction to the fabrication and use of materials
EA2	Application of engineering principles to the solution of practical problems based upon engineering systems and processes
EA3	A structured introduction to industry under supervision and involving a range of practical assignments.
EA4	Specific preparation for a first responsible post and a period carrying responsibility for that post under decreasingly close supervision.

Table 7-12. Engineering application definitions from the Finniston report.

Finniston recommended that EA1 and EA2 should take place at the undergraduate level, and specifically that EA2 might include a section on Business and Finance covering, ‘Background to engineering as a business and its economics. Introduction to balance sheets, costing and budgeting, marketing, selling and contracts, the value added concept and product life cycles.’. While claiming not to be prescriptive about course content, IEE accreditation procedures clearly point the universities in a direction that encourages the teaching of business awareness. However, judging by the responses to the academic questionnaire, these recommendations have not yet been adopted by many of the HEIs questioned.

Ensuring that the EA1 and EA2 skills are taught, by applying pressure to HEIs using the accreditation process, is far simpler than ensuring that recently graduated engineers follow EA3 and 4 to become ready for corporate membership. In recent times this has been

encouraged by approval of company training schemes to give a fast route to chartered status and by the introduction of 'Continual Professional Development' (CPD)

Using CPD, members of the IEE registered on the scheme can build up points for particular training and development activities, and so are able to certify that their training is progressing year by year (IEE, 1995).

7.4.4 The role of the 'Technology Champion'

The aim of the university questionnaire and the research into the role of the IEE was to ascertain the degree to which graduates could take the role of 'technology champion'.

A technology champion is somebody who is able to recognise the potential of an emerging technology and champion its adoption within an organisation. The champion must not only be able to consider technical aspects, but must be able to present the costs and benefits of adoption of a technology to his peers and to the senior management of an organisation. Senior management will often be involved in the approval process for the capital spending and product development spending necessary in adopting a new technology such as ASICs. The skills necessary to be a successful technology champion are summarised in *Figure 7-3*. These skills include:

- The technical skills (e.g. design skills) necessary to evaluate and work with the technology and communicate with technical peers
- The business skills (e.g. business planning) to be able to analyse the technology in relation to the company's strategic goals and communicate this to senior management

- The commercial skills (e.g. price negotiation) to be able to bring a new technology into a company from different suppliers who may use different business models to those normally used by the company's suppliers

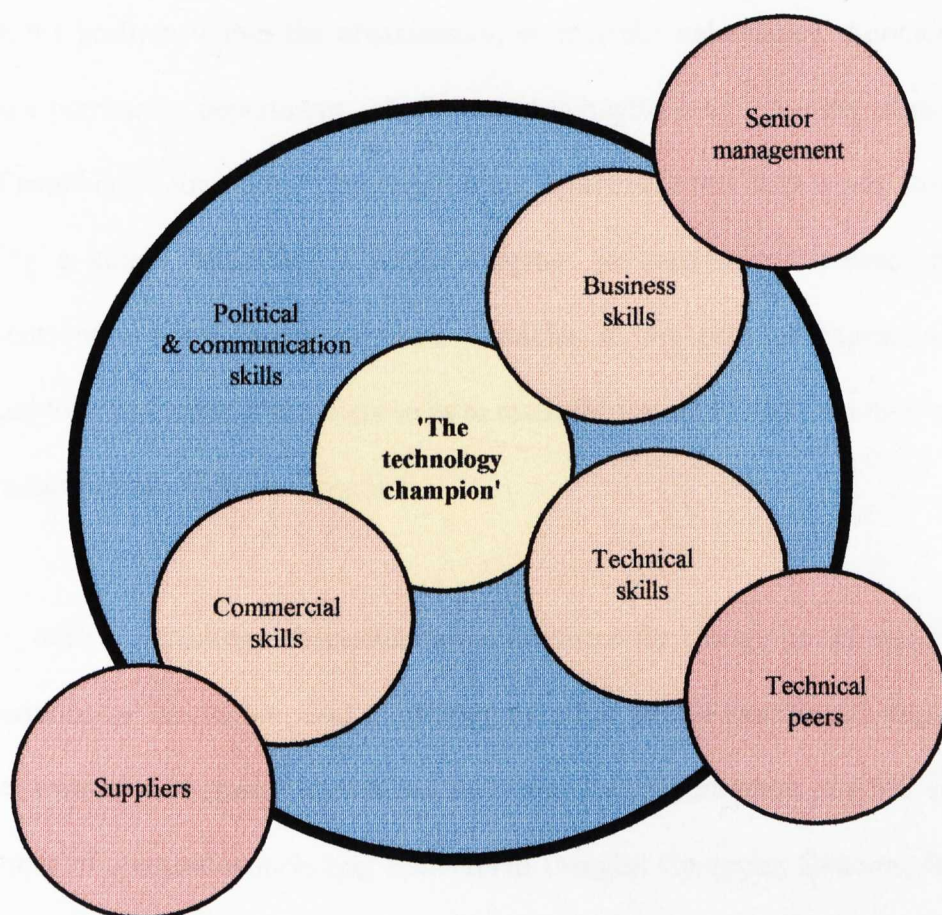


Figure 7-3. The 'Technology Champion'

The role of technology champion is a difficult one to fill. Clearly, technical, business and commercial skills will all be important in order to communicate and negotiate with other interested parties, but equally important will be the individual's political and communication skills. The adoption of a new technology can have far-reaching

implications for a company, and may meet with political opposition from those with a vested interest in the status-quo.

For example, an older engineer with outdated skills but a wide network of contacts within an organisation might try to resist the introduction of a new technology in order to maintain his position within the organisation, or to avoid redundancy. Another example might be a purchasing department, which is used to buying a wide variety of parts from a range of suppliers, being told by the engineering department that they would from now on be buying a single part from a single supplier. In such circumstances, purchasing departments have been known to place obstacles in the path of engineers who are attempting to introduce new suppliers so as to resist the introduction of the new technology and so preserve their traditional position.

However, once a technology champion exists, the force for change can become strong. In the experience of the author, and a number of other people questioned regarding this approach, examples of change agents had been seen causing adoption of ASIC technology in a number of companies including McDonnell Douglas Computer Systems, BICC Data Networks, and Neeve Electronics.

7.4.5 The 'Technology Champion' as a 'Change Agent'.

This role of Technology Champion discussed above is similar to that of 'Change Agent' discussed in a number of texts on change management (Spence, 1994). Spence considers that the change agent has a changing role over time which is shown in *Figure 7-4*.

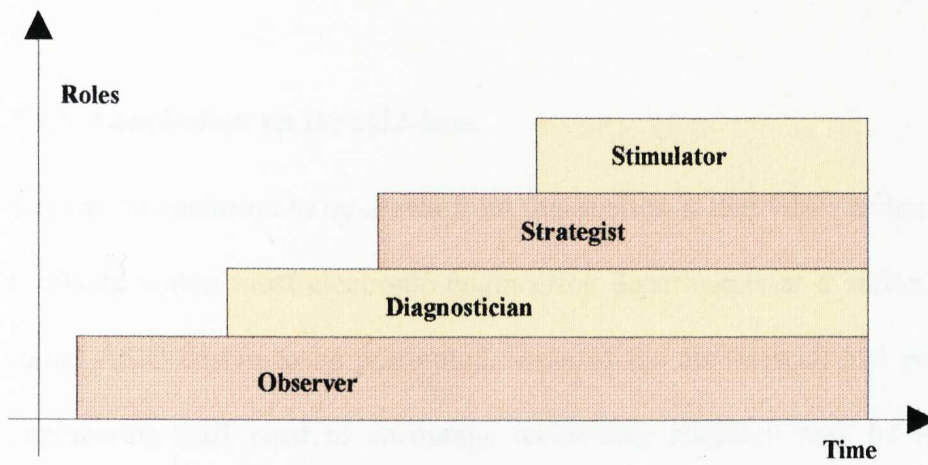


Figure 7-4. Roles of a change agent over time

Although Spence considers that a change agent is normally somebody from outside an organisation, the roles outlined apply equally to somebody within an organisation seeking to make a significant change (such as the adoption of a new technology).

The role begins as observer, during which time the change agent needs to analyse a current situation before being able to propose any changes. They must then become diagnosticians, able to understand a position and suggest changes that are likely to be practically implemented. The next role is that of strategist, which consists mainly of planning and policy making. The successful strategist must be able to identify a number of available routes to a goal, and propose the most likely to succeed. Finally, as stimulator, the change agent must motivate those around him to want to make a change, and to carry that change through to a successful conclusion.

As discussed elsewhere, the role of change agent is a particularly difficult one to fill, as it requires a high degree of technical, commercial and political skill to be successful.

7.4.6 Conclusions on the skill-base.

The main conclusion to be drawn from this section is that while technical skills should be available within most electronic engineering departments at a sufficient level to enable initial ASIC design to be performed, some of the commercial and political skills which engineering staff need to encourage technology adoption may be less evident in UK companies, and are not being included in engineering degree courses in spite of pressure from industry through the IEE.

7.5 *Insufficient Production volumes.*

The lack of sufficient production volume is often cited as a major reason for non-adoption of ASIC technology, and although this may be true for some of the technologies with higher NRE charges (e.g. cell-based ASICs), it is not considered to be true of the lower entry-cost technologies (e.g. programmable technologies such as FPGAs). In order to ascertain the break-even volumes for particular technologies it is useful to take a sample design and calculate the cost its development using a number of alternative technologies.

7.5.1 *Cost analysis of a sample design.*

In order to understand all of the cost implications of using ASIC technology it is necessary to consider more than the component cost of the ASIC and the alternate solutions. Many of the cost benefits of using these technologies come from the knock-on effects such as:-

- Lower manufacturing costs.
- Lower test costs.
- Smaller power supplies.
- Fewer or smaller PCBs.
- Fewer connectors.

For the sake of illustration a sample design will be used. This is identical to that used in the DTI's 'Custom Circuits Seminar' (Ivey, 1994) extended to compare additional technologies, and to consider a new product rather than the re-design of an existing one. If implemented in discrete components, the sample design is a four PCB sub-system which contains around 200 discrete logic chips (e.g. 74xx series TTL). It is assumed that 180 of

the devices can be integrated into an ASIC and that this leads to the four PCBs becoming a single PCB implementation. A production volume of 10,000 is also assumed.

When applied to the sample design the respective costs are shown in *Table 7-13*.

	Discrete	FPGA	Gate-array	Cell-based
Logic devices	36.00	45.00	12.00	8.00
PCBs & connectors	80.00	27.00	27.00	27.00
Assembly	3.75	0.06	0.04	0.04
Test	3.33	1.67	1.67	1.67
Total cost	123.08	73.73	40.71	36.71
Board level savings	0	49.35	82.37	86.37
Other savings (e.g. psu etc.)	0	13.00	15.00	15.00
Total system savings	0	62.35	97.37	101.37

Table 7-13. Example product costing.

However, in order to generate break-even figures, the relative cost of implementing these technologies must be taken into account. In general, the major costs are those of suppliers

NREs and any additional engineering time required over and above that used in the discrete design, for example in higher levels of simulation.

For the sake of this calculation, engineering time has been assumed to have a cost of £60,000 per man year including overheads (IEE, 1994). Other secondary costs such as reduction in PCB layout time could be taken into account, as could the whole-life cost reductions due to increased reliability, but these are more difficult to quantify. The total cost of the development is then amortised over the expected production run with the results shown in *Table 7-14*.

	Discrete	FPGA	Gate array	Cell based
Per-unit savings at 10k off (see above)	0	62.35	97.37	101.37
Suppliers NRE	0	0	20,000	40,000
Other expenses	0	0	15,000	25,000
Total expenses	0	0	35,000	65,000
Total gain (loss) 100 off	0	6,235	(25,263)	(54,863)
Total gain (loss) 500 off	0	31,175	13,685	(14,315)
Total gain 1k off	0	62,350	62,379	36,370
Total gain 10k off	0	623,500	938,700	948,700
Total gain 100k off	0	6,235,000	9,702,000	10,072,000

Table 7-14. Amortisation of development costs over volume manufacture.

The conclusion from these figures, for this design example, are clear. The use of a simple ASIC technology such as FPGA gives immediate savings over a discrete implementation even at volumes of less than 100 pieces. At around 1000 pieces it becomes more economic to use gate-array, and at around 10,000 pieces the lower cost of a cell-based part makes it more economic. This is summarised in *Figure 7-5* below:-

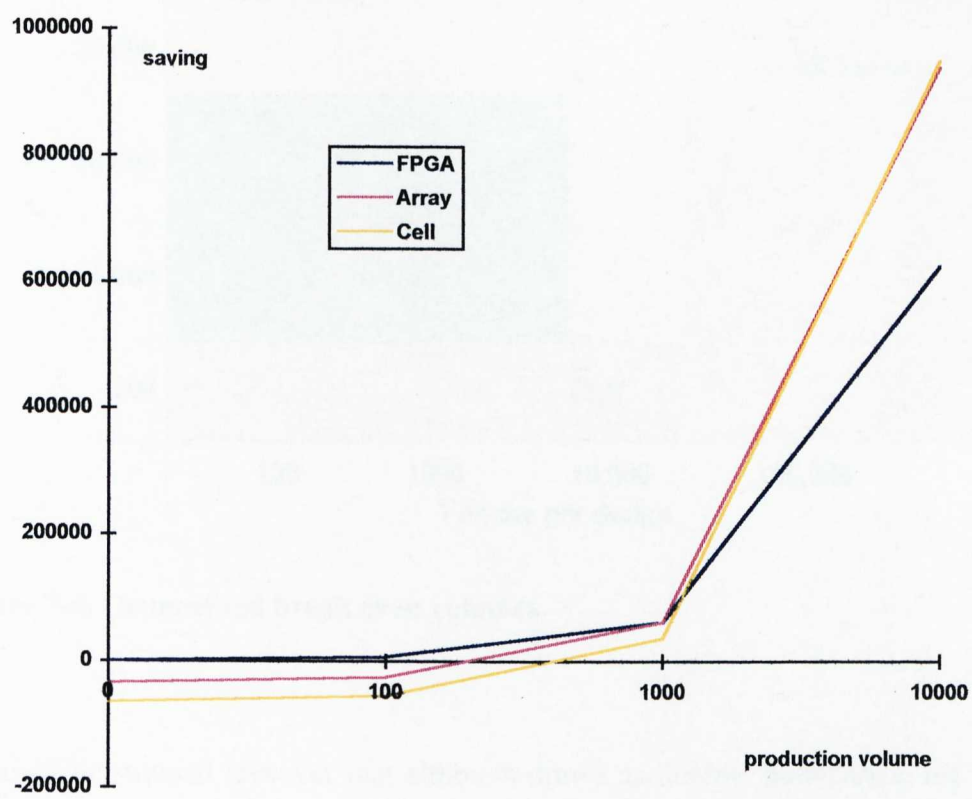


Figure 7-5. Savings for ASIC types with volume.

7.5.2 Generalised break-even volumes.

The above indication is specific to a particular design, and the break-even volumes would vary for different chip sizes and design types, but this approach can be used to produce

generalised figures for the different technologies. If this costing approach is applied across the range of technologies the diagram below (*Figure 7-6*) results (Ivey, 1994).

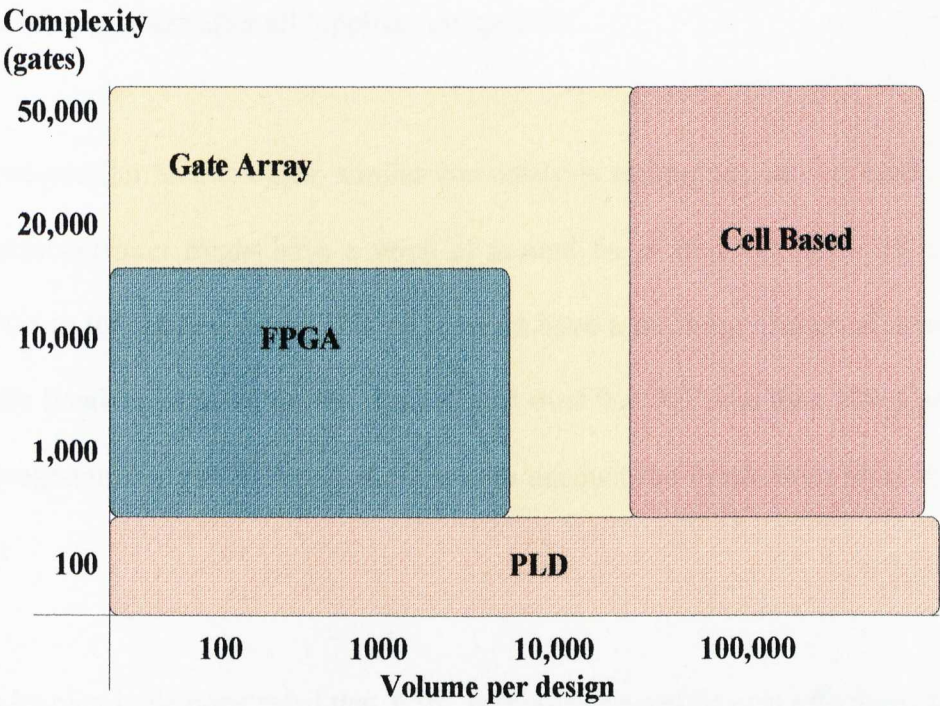


Figure 7-6. Generalised break even volumes.

It should be stressed however that although drawn as distinct boundaries, the boundaries are in fact ‘fuzzy’. In some applications it may be cost effective to consider high levels of integration for low product-volumes when the complete product is considered (e.g. flight hardware for satellites where final equipment weight is all-important).

This fuzziness is compounded by the emergence of some intermediate technologies such as the Xilinx ‘Hardwire array’. This is a masked technology which is simply a copy of the Xilinx SRAM based FPGA technology with the SRAM cells replaced by masked connections. In this way users can migrate quickly from an FPGA prototype to a masked

device which, although not as effective in its use of silicon area as a gate-array, is considerably smaller, and hence cheaper than the FPGA that it replaces.

It is necessary to take each application in isolation and produce a cost model appropriate to it. The technologies are after all 'application specific'.

For microcontroller technologies, similar cost-analysis techniques can be used. A typical small microcontroller might have a price of around £4 in its OTP form and a price of around 50p in its masked form. This part would have a masking charge of about £2,000 making the break-even point for the masked part over the OTP less than 600 pieces. If the cost of programming the OTP part is taken into account the break-even level drops even lower.

So it can be clearly demonstrated that ASIC technologies can be cost effective at very low volumes, and certainly at the volumes produced by many SMEs. It is concluded therefore that when SMEs claim that insufficient production volumes are a reason for non-adoption, they are mistaken in their assumptions. Interestingly, in the survey discussed in Chapter 4 (Shortland, 1991) there is an example of a company claiming that their volume (over 30,000 pieces per year) was insufficient to consider using an ASIC.

7.5.3 Restrictions on minimum quantity in masked devices.

The break-even figures shown in this chapter for masked devices suggest that they can be cost-effective at fairly low quantities. However, this makes the assumption that such quantities will be delivered by semiconductor suppliers. While multi-project wafers and other similar techniques go some way to make this possible, the attitude of semiconductor

vendors to low-volume orders is also critical. At various times during the course of this study, the world's semiconductor fabrication plants were working at close to their maximum throughput, and as a consequence, semiconductor manufacturers were 'cherry picking' the more lucrative contracts. This led to significant difficulties in finding sources of masked devices except in large quantities, particularly for mixed-signal devices. This concern was reflected in the survey of design-houses performed by the Semiconductor Businesses Association in 1996 (SBA, 1996). In this survey over 40% of respondents claimed that minimum order quantities were causing a problem to potential clients. Limited foundry capacity, particularly within the UK, was also identified as a significant concern.

7.5.4 Conclusions on volume requirements.

It can therefore be illustrated that insufficient production volume does not represent a real barrier to entry to all but the most expensive ASIC technologies (e.g. masked cell-based devices). Technologies exist with very low entry and design costs which can be easily recovered over relatively modest production runs.

7.6 Risk of failure.

Risk of failure is a little more difficult to quantify than the other reasons for non-adoption. Risks increase with the complexity of the technology adopted. For well established technologies (e.g. digital ASIC) most designs can be shown to be 'right first time' (Ivey, 1994). This is certainly borne out in the author's experience. But with the more complex technologies the risks are higher. The XXX Ltd. case study discussed in *Chapter 6* shows that a risk of failure still exists, but these risks can be reduced or eliminated.

The major factor aiding the engineer in producing 'right first time' designs is the large number of CAE software tools that are available to simulate and verify the design prior to its fabrication. It was the failure to use a consistent set of tools that was a major contributory factor in the case of XXX Ltd discussed above. If used correctly, these tools can provide a high level of confidence that the ASIC will function as specified. The behaviour of the ASIC, or the complete product, can be simulated across the complete spread of production variations and environmental conditions that the product will encounter. This is a far more rigorous approach than producing a laboratory prototype using typical components, and can in consequence reduce the occurrence of problems throughout the product's lifetime.

An interesting view on the perceived nature of the risks in using ASICs came in discussing potential uses of ASIC technology to replace electromechanical controllers with a white goods manufacturer. Their Chief Engineer commented, "With our usual electromechanical approach, at least if it doesn't work we can bend the metal a bit and make it usable. You can't do that with an ASIC can you". In other words, he was concerned about the costs, timescales and levels of scrap that would result from a faulty prototype or early production

run. But even here, the conceptions are incorrect. It is usual in applications where there is a degree of uncertainty to make parts of even masked ASICs programmable. For example, in the TRACKER device discussed in *Chapter 3*, many of the parameters used in the demodulation scheme are loaded from a microcontroller into registers within the cell-based ASIC. This allows exactly the sort of ‘metal bending’ required by the Chief Engineer above. Had any problems with the modulation scheme been identified in testing, various parameters of the algorithm could have been ‘tweaked’ in much the same way as minor changes to metalwork are made in a mechanical prototype.

7.6.1 Conclusions on risk of failure.

So in consequence, if correct design approaches and simulation methods are used, the rigorous design proving performed on ASIC devices prior to fabrication can in fact reduce the risk in a design rather than increase it. It is also possible to reduce the risk of unknown systemic effects causing problems by making critical parts of masked devices programmable. Once again, the perceptions held by many potential users regarding the risk of failure when using ASIC devices are incorrect.

7.7 Lack of second source.

The significance of this problem seemed to have diminished between earlier surveys and the user-survey performed for this study, but it did still appear as a reason in some responses. This section aims to ascertain whether lack of a second source for a particular ASIC device is still a problem that might prevent adoption of the technology.

7.7.1 Multi-sourcing an ASIC

In the early days of ASIC technology, a user was faced with considerable pressure to decide on a particular ASIC technology and supply company and to continue to use that company to supply the ASIC for the remainder of the life of the product. This was due to a number of major reasons:

- ASIC technologies were unique to a particular silicon-vendor, so transfer of a design involved redesigning the circuit to use the building-blocks available in the new technology with all of the inherent risks of what is essentially a new design.
- Design tools were sometimes unique to a particular vendor, so design transfer would involve learning how to use a new tool-set, and might include the purchase of a new tool-set.
- The design of the new chip would require the payment of a new NRE charge, and NRE charges were relatively higher than they are today.

- Chips sometimes contained large functional blocks designed by the silicon vendors (e.g. processor cores). As the silicon vendor owned the Intellectual Property Rights (IPR) of these blocks, it was not possible to transfer them to the second-source supplier.

The problems inherent in single sourcing have diminished in recent years. This is due mainly to the factors discussed below.

7.7.2 Second source agreements between vendors.

With standard IC parts, the volumes produced often warrant a vendor producing an equivalent part to that of a competitor, either with or without their consent. This was generally not the case with ASIC technologies. However, as ASICs became accepted in military products, their designers began to insist on second sources either to guarantee local supply or to guarantee supply in a disaster recovery situation. This led to a number of agreements which, although poorly publicised, allowed direct mask-transfer between vendors and so gave vendors the ability to manufacture each others ASICs. There was often a commercial barrier placed in the way of a user wishing to take this route, but nevertheless the routes existed. The situation developed further in the 1980s as the cost of developing new silicon technologies became prohibitive even to the largest silicon vendors. This led to a number of joint technology development programmes, and consequently to an obvious route to second sources. Examples of this include developments between LSI Logic and Toshiba, and between LSI Logic and AMD.

7.7.3 Demise of vendor specific design tools, or vendor specific libraries on standard tools.

Early ASIC families relied heavily on design tools produced by the eventual silicon vendor (e.g. LSI Logic's LDS, Fujitsu's FAME). These tools were specific to the design of one vendor's products, and transfer to another vendor involved installation, learning and redesign using a completely new toolset. Even as new, generic CAE platforms emerged (e.g. Daisy, Mentor, Valid) the cost of developing different libraries for each system meant that silicon vendors generally picked one or two CAE suppliers and concentrated their library development effort on those platforms. This problem has been alleviated in recent years by the emergence of two 'standard' library languages; Verilog, using XL as its description language, and the formation of the VITAL group, who are attempting to use VHDL as a standard for developing ASIC libraries.

This will mean that libraries and simulation results are transportable across a wide variety of target CAE systems, so that users will not be restricted to libraries developed for a particular toolset. As the sophistication and cost of developing CAE software increases, silicon vendors have withdrawn from the CAE market, leaving even final sign-off simulation to be done on generic platforms (most usually Cadence).

7.7.4 Emergence of synthesis tools.

The emergence of synthesis as a design methodology has enabled simple and speedy re-targeting of ASIC designs between families to be realisable. In very recent years high-cost synthesis tools such as Synopsis (the industry standard) have been joined by a number of lower-cost tools (such as Transgate - from transEDA). In consequence, the cost of re-

targeting has been significantly reduced, and the threat of it is often sufficient to prevent a silicon supplier from trying to exert the price pressure often associated with single sourced devices.

These advanced design-tools are now becoming widely used, at least in design-houses. The SBA survey discussed earlier (SBA, 1996) established that the use of HDL and synthesis tools was fast approaching the level of use of schematic capture tools as the favoured design-entry technique in the UK, and that it had overtaken schematic entry in the design houses of mainland Europe. Similar surveys undertaken in the more general design community (Joselyn, 1996) suggest that around 40% of designers are using HDLs and logic synthesis in the design of programmable logic. Using these tools to transfer an ASIC device from one supplier to another can have very low costs. In an interview with *Electronics Weekly*, Orbit Semiconductors claimed that their NRE charges for re-targeting an existing device were in the range of zero to \$10,000 (Anon, 1995:2).

The emergence of high-level design languages and synthesis tools has also led to the establishment of the so-called 'chipless chip companies'. These are companies who design chips or functional blocks in a HDL format and then sell those functional blocks to users for incorporation in larger designs. Such companies include Advanced RISC Machines (ARM), and 3Soft and Systolic Technology, who have recently been acquired by the CAE company Mentor Graphics. Interestingly, Mentor Graphics see the sale of intellectual property as key to their future business success (Mentor, 1996). A knock-on effect of this approach is that large functional blocks are available which are independent of silicon vendors, and can easily be re-targeted to a new technology.

7.7.5 Conclusions regarding second sourcing.

So, it can be shown that the second sourcing of ASIC devices no longer presents the level of cost and risk that it once did. Routes to second sources exist at a relatively low cost, and the inherent risks are no greater than companies routinely face with other technologies (e.g. plastic molding tools). The emergence of more sophisticated CAE tools has had a great influence in making these changes. Again, it would appear that the problem perceived by potential users of ASIC technology has its roots mainly in history and myth.

7.8 General conclusions on user reasons for non-adoption.

At the beginning of this section, a number of user perceptions regarding ASIC technology were identified by the use of a specific questionnaire and reference to previous work. Each of the major reasons cited by potential users of ASIC technology has been analysed, and it has been shown that many of these perceptions are misconceived.

However, this does not make the reasons for non-adoption any less real in the minds of the potential user, or any less powerful in preventing them from adopting ASIC technology. It has long been understood that a user's perception of the features of a product are as highly influential in their buying decisions as the reality of the features (Skinner, 1990). Indeed it is this that sustains the advertising industry. For example, at the time of writing, there was a perception that British beef was prone to carrying a disease (BSE), and although little scientific evidence suggested that such a perception was well-founded, the market for beef was severely reduced. Clearly, perception is as important as fact in influencing a market.

If we assume that respondents to the user questionnaire were replying truthfully, and adoption is to be increased, ways must be identified to overcome these incorrect perceptions before adoption will even be considered.

8. Models for evaluating the causes of adoption and non-adoption.

It can be seen from the research detailed in earlier chapters, that the reasons most often cited by potential users for non-adoption bear little basis in fact. However, unless non-users are being deliberately misleading, which we must assume they are not, those perceptions are inhibiting the uptake of the technology.

In deciding on the most appropriate models to use for the analysis of the situation, it is useful to review two major types of situation or problem and to classify the adoption of ASICs as one or the other. An Open University course on change management (Open University, 1986) defines these two classes of problem as 'hard' and 'soft'. The characteristics of the two types are shown in *Table 8-1*.

Hard Problems	Soft Problems
One clear solution	No one clear solution
Solution can only be one thing	Resolution can be one of many things
Know what the problem is	Not sure what the problem is
Know what needs to be known	Not sure what needs to be known
Clear method of working it out	No obvious method of working it out
Structured	Unstructured
Clear-cut	Messy

Table 8-1. Characteristics of 'Hard' and 'Soft' problems

As examples, it can be seen that a mathematical problem and improving the operation of a production line might be classified as 'hard' problems. Such problems are clearly defined and have a single correct solution. There then follows a whole spectrum of situations ranging from the purely 'hard' to the purely 'soft' (e.g. the introduction of a new political system).

One problem with this method of classification is that very few problems can be considered to be completely 'hard'. Almost any problem that one might consider will have some human element to it which is likely to give it some characteristics of the soft type. Even the example used above (changing a production line) would normally have some human implications and so would start to become 'messy'.

In general, it may be assumed that most problems involving diverse sets of people are to some extent 'soft'. The diverse sets of opinion and interest inherent in such situations means that there is rarely a single clear solution, and even if one should exist it would be unlikely that all those involved would accept it.

The wide range of reasons and perceptions described earlier in this study suggest that ASIC adoption is not a hard problem and so should be regarded as soft. This difficult and often subjective mixture of fact and perception lends itself to analysis using system based methodologies. A number of such models are used in this chapter.

8.1 Defining the system.

In order to use system methodologies it is useful to first define the boundaries of the system being considered. This system has already been identified and described in *Chapter 5*, and is repeated in *Figure 8-1*.

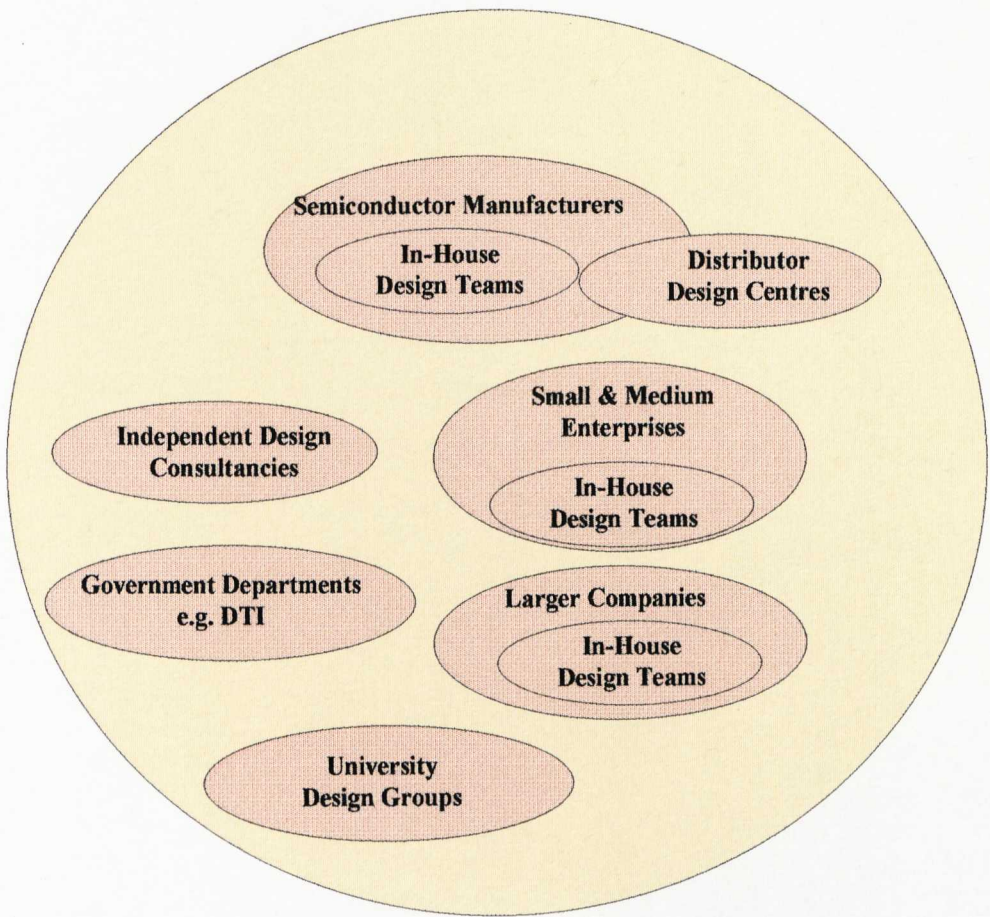


Figure 8-1. *A systems map of the UK ASIC market.*

This systems map shows the major groups that will be considered in this analysis. Further details of each group is given in *Chapter 5*. As with most analyses using this method, the major problem is one of deciding which areas lie within the system boundary and which outside. Once that decision is made, the situation becomes more bounded rather than being completely open-ended.

8.2 Multiple-cause diagram of retarding forces

In an attempt to resolve the systemic problems identified earlier in this study, the following multiple cause diagrams are presented as an initial summary of the forces at work in the system. *Figure 8-2* summarises forces retarding adoption, while *Figure 8-3* summarises forces supporting adoption.

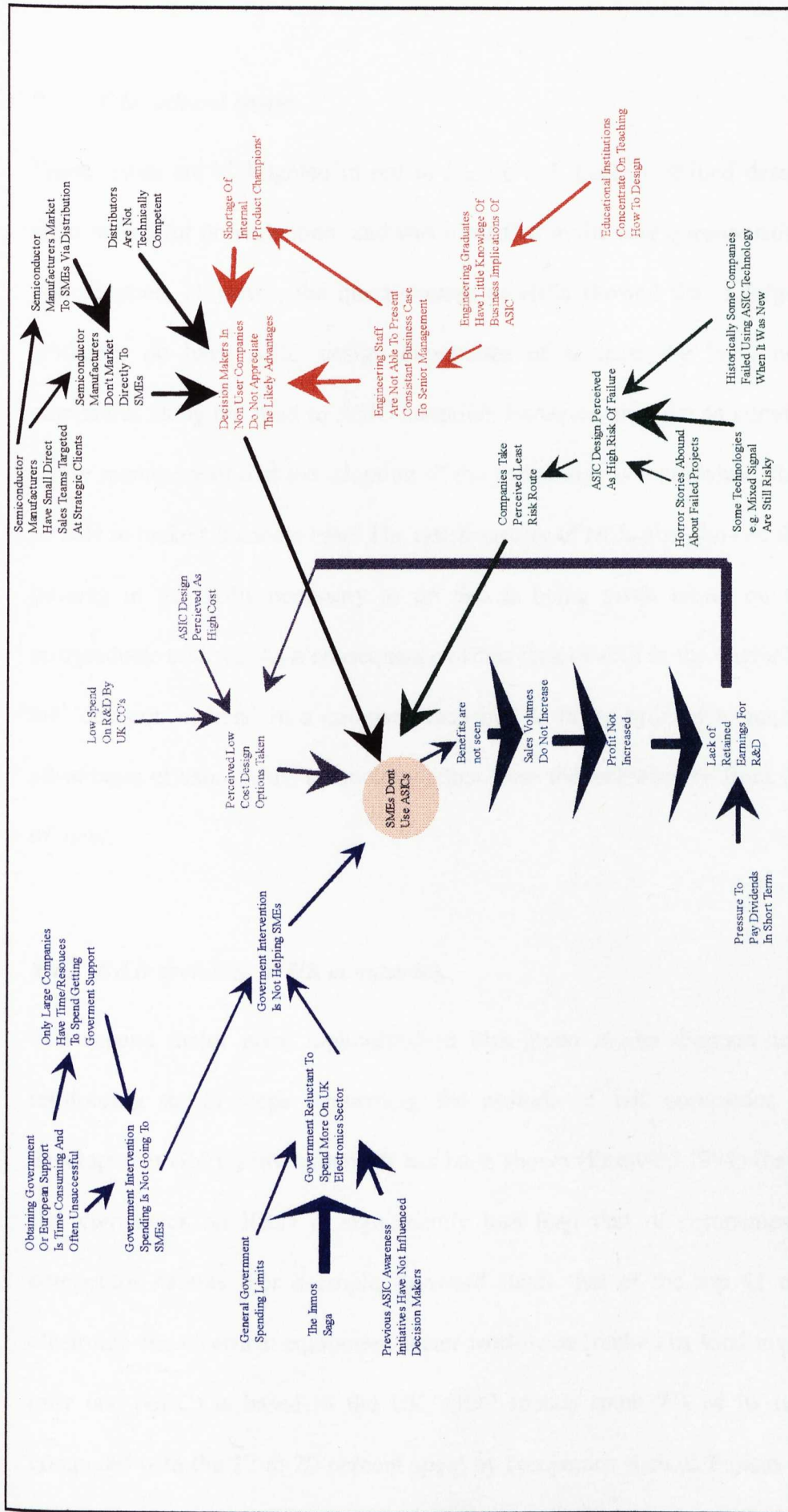


Figure 8-2. Forces against adoption. Multiple cause diagram

Each of the contributory areas shown in *Figure 8-2* will now be considered.

8.2.1 *Educational issues.*

These issues are highlighted in red in *Figure 8-2*. Lack of skilled designers is an often cited reason for non-adoption, and was identified in the user questionnaire as a reason for non-adoption. However, the questionnaire of HEIs showed that a large number of UK graduates do have ASIC design experience of at least the level necessary to start companies along the road to ASIC adoption. However, in order to convince a company's senior management that the adoption of the technology is worthwhile, the engineers must be able to make a business case. The questionnaire of HEIs also showed that little effective training in the skills necessary to do this is being given either on undergraduate or postgraduate courses. As a consequence of this lack of skill in the engineering community, the 'decision makers' in a company may not be being brought to appreciate the likely advantages of using ASIC technology either from the technical, or from the business point of view.

8.2.2 *R&D spending in UK companies.*

The second major area, highlighted in blue-green in the diagram is a circular, self reinforcing set of steps concerning the attitude of UK companies to research and development (R&D) investment. It has been shown (Kenward,1994) that the spending of UK companies on R&D is significantly less than that of companies in some of its competitor nations. For example Kenward states that of the top 41 companies in the electronic and electrical equipment sector worldwide (ranked by total investment in R&D) only one (GEC) is based in the UK. GEC spends some 7% of its turnover on R&D compared with the 12 to 20 percent spent by companies such as Fujitsu (Japan), Ericsson

(Sweden), and Amdahl (USA). Kenward does however concede that his results are based on the reported results of large companies rather than those of unlisted organisations where pressure to meet the short-term needs of the stock-market might not be as strong. However, a survey performed by the Semiconductor Businesses Association (SBA, 1996) suggests that a low level of R&D spending is also evident in the SME sector.

This reluctance to spend on R&D is echoed in a reluctance of R&D departments to spend money on training their staff in emerging new technologies, and even greater reluctance to spend money on business skills training. Training in R&D departments is often perceived as a cost rather than an investment, and is one of the first areas to be cut in times of recession.

As a result of this tight financial control on R&D, companies are pressured into staying with what they perceive to be low-cost, low-risk technologies. As this study has demonstrated from the user questionnaire, ASIC technology is seen as both high-cost and high-risk. As a result of the lack of adoption of new technology, many of the products produced by UK companies are mediocre when compared to those of their more adventurous competitors. The inevitable result is mediocre sales, and a consequent lack of earnings which might be retained in order to fund further R&D. In addition, it is widely accepted that the UK stock-market takes a very short-term view of its investments, requiring the payment of dividends and generation of profit in the short-term to take a higher priority than long-term investments, so further reducing a company's ability to invest in its future products.

The multiple cause diagram shows the relationship as a self perpetuating loop. Clearly this loop needs to be broken if progress is to be made towards adoption of ASIC technology.

8.2.3 Manufacturers marketing issues.

The third major area identified (highlighted in black on the diagram) relates to the relationship between the major semiconductor manufacturers and the SME user. The major semiconductor companies generally have fairly small direct salesforces who concentrate on major accounts. For example, in 1994 LSI Logic employed about 5 direct sales people to cover the whole of the UK, and NEC employed just one.

The interface between the large semiconductor manufacturers and SMEs is traditionally covered by their appointing distributors who then interface with the SMEs. This approach is generally acceptable in the promotion of standard products, where the semiconductor manufacturer can write highly informative data books and maintain an arms-length contact with SMEs. The distributor has simply to take and process orders. For some more technically advanced products, distributors appoint Applications Engineers (AEs), but this position has rarely attracted high caliber engineers, and UK AEs have gained a poor technical reputation, acting often as simply a conduit for passing problems back to the manufacturer. This process is discussed in some detail in *Chapter 6*.

When initially considering the promotion of ASICs to SMEs, many manufacturers assumed that their normal distribution route could be adopted, and so distribution channels were established. However, the situation is considerably different to that for standard products. The buyer is generally an engineer rather than a purchasing department, and they

must be confident that their technical problems are understood. Application Engineers proved unable to do this. In addition, the selling cycle for an ASIC design is much longer than for standard parts. In the author's experience it generally takes over a year from first meeting to development order, and the chip is unlikely to be in volume manufacture (and hence earning commission for a distributor) for at least a further year following development and product launch. Distributors are simply not able to support this lengthy and highly technical process. Some have tried to set up design groups to perform ASIC designs and so decrease the time to generating revenue, but the results were often disastrous for reasons of culture and management (this was discussed more fully in *Chapter 6* with the XXX Ltd. Case study). Most design groups set up in this manner have since closed.

The result of this approach is that ASICs are not effectively marketed to SMEs by the major semiconductor companies. This reinforces the position that decision makers are not made aware of the benefits of ASIC technology, and so are not inclined to adopt it.

8.2.4 Risk issues

Issues concerning the risk involved in using ASIC technologies (highlighted in green) have a large part to play in the adoption process. At the time when today's senior engineering managers were practising engineers, ASIC technology carried significantly higher risks than it does today. Horror stories of failed ASIC developments abounded, the design-tools were unreliable, and a number of innovative companies failed to successfully adopt ASIC technology. Even today, some ASIC technologies can be risky (e.g. mixed-signal technologies). The upshot of this is that decision makers still regard the technology as

risky. In any business, risk is seen as something to be avoided if possible, and consequently the technology is not adopted.

8.2.5 *Government intervention issues.*

The last major area in the diagram is that of government intervention (highlighted in blue). In *Chapter 5* the history of the Alvey Programme was discussed. This programme is typical of microelectronics programmes undertaken by governments prior to recent programmes such as Microelectronics in Business and Europractice. The older programmes, and much of the UK and European grant support (e.g. The ESPRIT programme) were aimed at increasing the availability of technology through funding technology providers (chip fabrication plants and the like). In consequence, much of the available finance was used to subsidise the development of new, 'state of the art' technologies rather than the promotion of existing technologies to potential users. This approach does not in itself constitute an industrial policy capable of increasing adoption among SMEs. In addition, the highly bureaucratic nature of the application process, the need to secure multiple (often overseas in the case of EU schemes) partners, the likelihood of failure to gain funding, and the reluctance of schemes to support other than pre-competitive developments made the effort involved in applying for support unattractive to all but a few brave SMEs.

One example of large-scale intervention which failed, and was to make successive UK governments more reluctant to become involved in microelectronics was the establishment of Inmos (McLean & Rowland, 1985). This company was established with a high degree of government support under the leadership of Baron and Peritz in 1978, shortly before the demise of the then Labour government. While responsible for a number of significant

developments in microprocessor technology (e.g. the Transputer) and high-speed static and dynamic memory devices, Inmos was unable to maintain sufficient investment in fabrication equipment or a high enough standard of production quality to remain viable. The company went through a protracted period of uncertainty before eventually being sold to SGS-Thomson who closed the manufacturing facility and eventually abandoned the technology.

8.3 Multiple-cause diagram of supporting forces

However, the forces at work within the system are not all negative ones. A number of recent developments have taken place which stand to support the adoption of ASIC technology, particularly by SMEs. These forces are summarised in the multiple cause diagram shown in *Figure 8-3*.

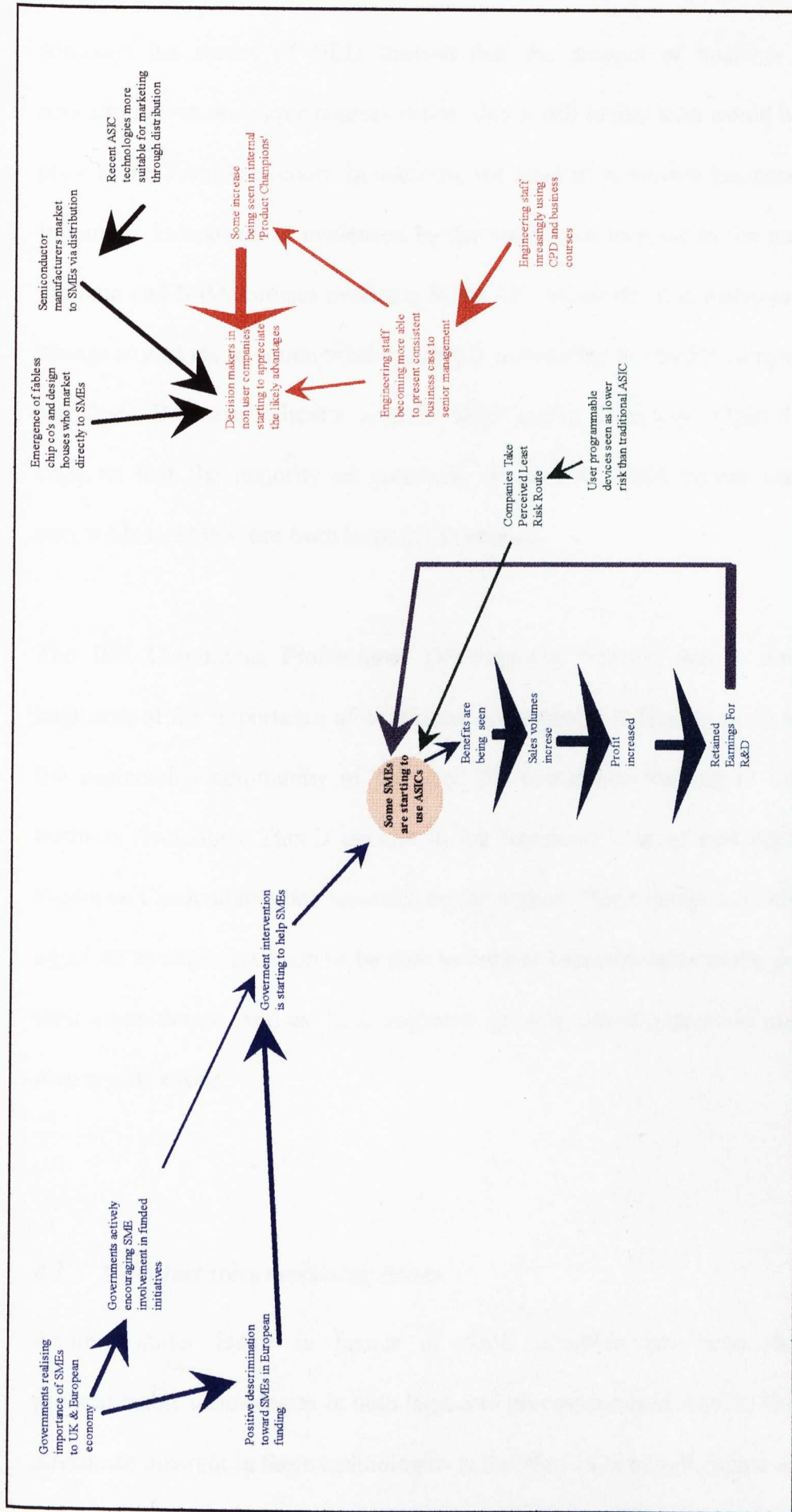


Figure 8-3. Forces supporting adoption. Multiple cause diagram.

8.3.1 Educational issues.

Although the survey of HEIs showed that the amount of business and commercial education given on degree courses is low, this is still higher than would have been the case prior to the Finniston report. In addition, the level of in-service business and commercial training is increasing, as evidenced by the significant increase in the number of business diploma and MBA courses available in the UK. However, it is questionable whether this change in attitude to commercial training is permeating to smaller companies. A review of the Open Business School's Alumni Membership Directory (Open University, 1996) suggests that the majority of graduates of the OU MBA course (arguably the most accessible to SMEs) are from large organisations.

The IEE Continuous Professional Development scheme, and a realisation amongst engineers of the importance of continued development is leading to an acceptance within the engineering community of the need for continuous training in both technical and business disciplines. This is evident in the increased level of post-appointment training shown on Curriculum Vitae reviewed by the author. These trends can only help to increase adoption as engineers learn to be able to present business cases to the decision makers in their organisations, and as these engineers grow to become decision makers within their own organisations.

8.3.2 Manufacturers marketing issues.

Another major factor in favour of ASIC adoption has been the emergence of programmable technologies in both logic and processor-based ASICs. The main marketing advantage inherent in these technologies is that they bear a high degree of similarity to the

standard parts that are easily sold through distribution. The entry-cost to using the technology is low, the level of technical support required is lower than for masked devices, and the perceived level of risk amongst informed users is also less than for more complex ASIC technologies. Consequently, traditional semiconductor marketing methods using distributors and application engineers are more suited than they were to masked ASIC marketing. As a result, more companies are getting onto the lower rungs of the ASIC ladder, and so starting to see the benefits of using ASICs in their products. This is evidenced by the continuing worldwide growth in programmable logic sales which are predicted to grow to over \$2Billion in 1997 (Parry, 1996).

Providing support for this process is adequate, the increase in use of programmable devices is likely to lead to successful products which can only act to reinforce the use of the simple devices and lead companies to consider more complex ASIC technologies. Such companies need to consider the more complex technologies to be simply a further step in ASIC adoption. This is being aided by the emergence of re-targeting tools which enable programmable solutions to be easily re-targeted to masked devices.

8.3.3 Government intervention issues.

In spite of inevitable criticisms, government schemes, in both the UK and Europe, are coming closer to the needs of the SME than they ever have before. Support grants have moved from solely supporting long-term and pre-competitive research, to supporting technology transfer and initial projects. MiB, SPUR, SMART, and EUROPRACTICE, discussed elsewhere, are all examples of this. All of these schemes concentrate on the

needs of small companies, as government has come to realise that such companies form a major source of employment, and the major source of growth in employment.

8.4 The nature of innovative developments.

In considering the perceptions of potential users it is important to realise that there is not one single overwhelming reason for non-adoption, but a whole range of smaller reasons which may be either real or imagined. This should be considered in relation to the types of innovative development that may be encountered in companies. These developments range from small incremental developments to major step-changes. (Gardiner and Rothwell, 1989). This is illustrated in *Figure 8-4*.

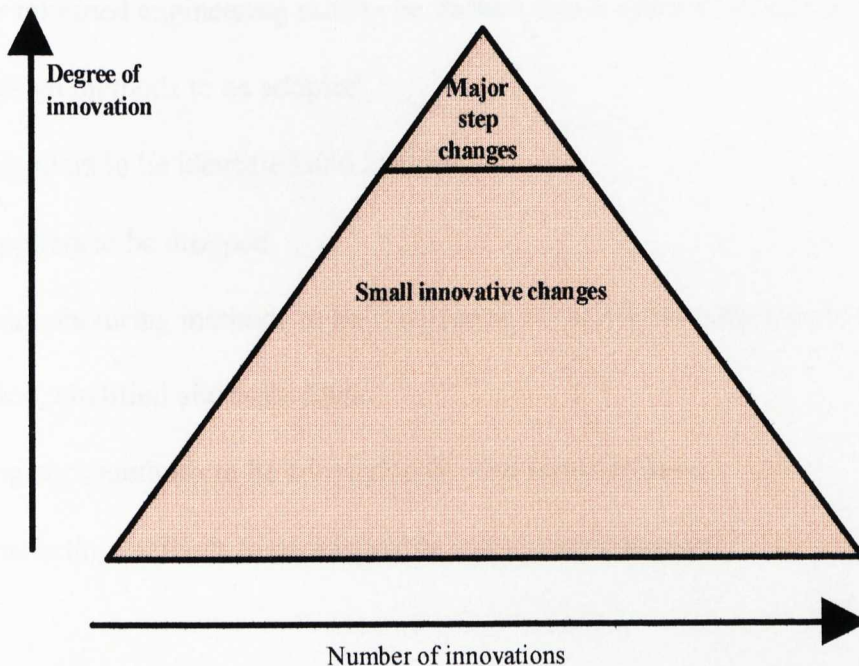


Figure 8-4. The nature of innovative developments.

Most innovative changes (over 90%) fall into the category of small innovative changes. They normally involve a minor change to a process, method or technology. Examples of this might be a migration from one plastic material to another for a molded part, or the adoption of a change to the setup procedure for a machine tool. The important thing to

note is that while they may be significant in a single area, they do not generally have major knock-on effects in other areas of the company.

Once a change, no matter how small in nature, starts to have knock-on effects, it should be considered as a major step change. If one considers the introduction of even a low-cost ASIC technology to a company that previously had no electronics in its products, the knock-on effects are significant. They can include:-

- New design tools to be identified, purchased and assimilated
- New or retrained engineering staff to be formed into a cohesive design team
- New design methods to be adopted
- New suppliers to be identified and qualified
- Old suppliers to be dropped
- New manufacturing methods to be introduced, or new subcontract manufacturers to be identified, qualified and assimilated
- New logistics methods to be adopted to fit with new suppliers
- New marketing methods to be adopted to support new products

Consequently, it is of little surprise that the adoption of microelectronic technology is treated with trepidation by new users. If adoption is to be encouraged, a means should be identified that allows the adoption to take place as a series of small incremental steps.

Methods of achieving this are discussed in *Chapter 9*.

8.5 Factors relating to innovation.

Spence (Spence, 1994) refers to a number of factors which may affect the likelihood of an innovation being introduced. These factors are illustrated in *Figure 8-5*.

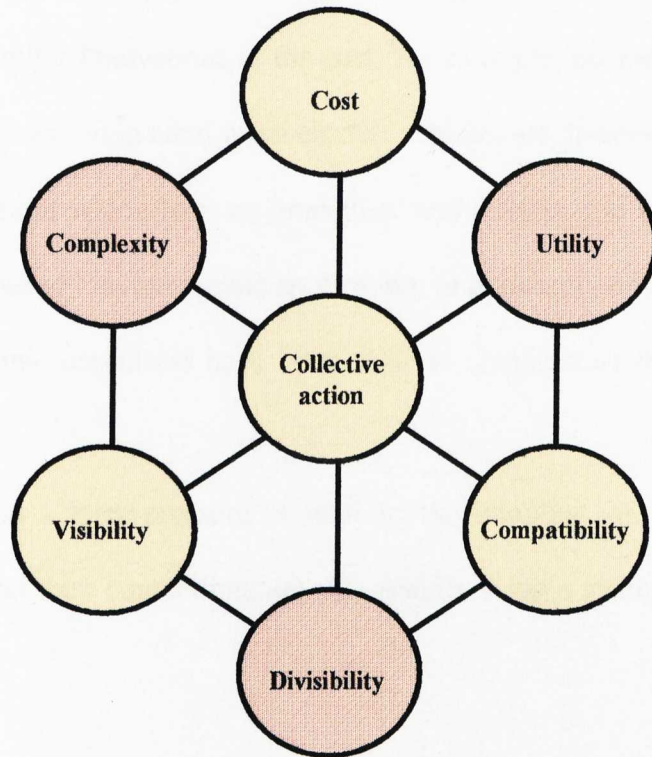


Figure 8-5. Factors relating to innovation

These factors may be summarised as:-

- **Cost** - A new product or process is more likely to be adopted if it is low cost irrespective of the size of the potential return
- **Complexity** - Ideas and practices that are relatively simple to understand are more likely to be adopted than those of greater complexity
- **Visibility** - An innovation is more likely to be adopted if it can be seen to work (for example, post-emergence weed killers are commercially more successful than the more

effective pre-emergence varieties because, by the time they are needed, the problem has become clearly visible, as has the effectiveness of the solution.)

- **Divisibility** - An innovation is more likely to be successful if it can be tried in part before complete adoption (putting a toe in the water)
- **Compatibility** - The view a person holds regarding an innovation is coloured by their experience of similar innovations in the past. For example, peoples view of the failure of the Sinclair C5 are often cited when electric vehicles are discussed.
- **Utility** - Innovations which have an immediate and obvious use will be more likely to succeed than those of less immediate application. (e.g. instant coffee was quick to catch on while electronic organisers have been slow to demonstrate their advantages over paper diaries.)
- **Collective action** - Peer pressure is vital in the adoption of innovation. When a company sees that their competitors are successfully using a technology, they are more likely to adopt it.

When these criteria are applied to ASIC technologies we can derive a number of additional reasons to explain the slowness of adoption.

Criterion	Status in relation to ASIC technologies
Cost	ASICs are perceived as having a high cost
Complexity	ASICs are perceived as a technically complex technology
Visibility	Success should be fairly visible, although perhaps not in product areas which traditionally don't use microelectronics
Divisibility	Traditionally ASIC adoption was all or nothing, but programmable technologies are changing this
Compatibility	Horror stories of failed ASIC developments are still prevalent in poorly informed sectors
Utility	This will be very application specific
Collective action	No peer pressure will be evident in sectors which have not begun adoption.

Table 8-2. Factors affecting innovation

It is clear that a number of reasons for non-adoption of ASIC technology can be identified using this adoption model. The model may also be used to check the validity of approaches used to increase adoption. This is pursued further in *Chapter 9*.

8.6 Adoption and communication

Spence (Spence, 1994) describes a route between initial need recognition and the adoption of a new situation which has become widely used in the discussion of innovation and adoption. This route is summarised in *Figure 8-6*.

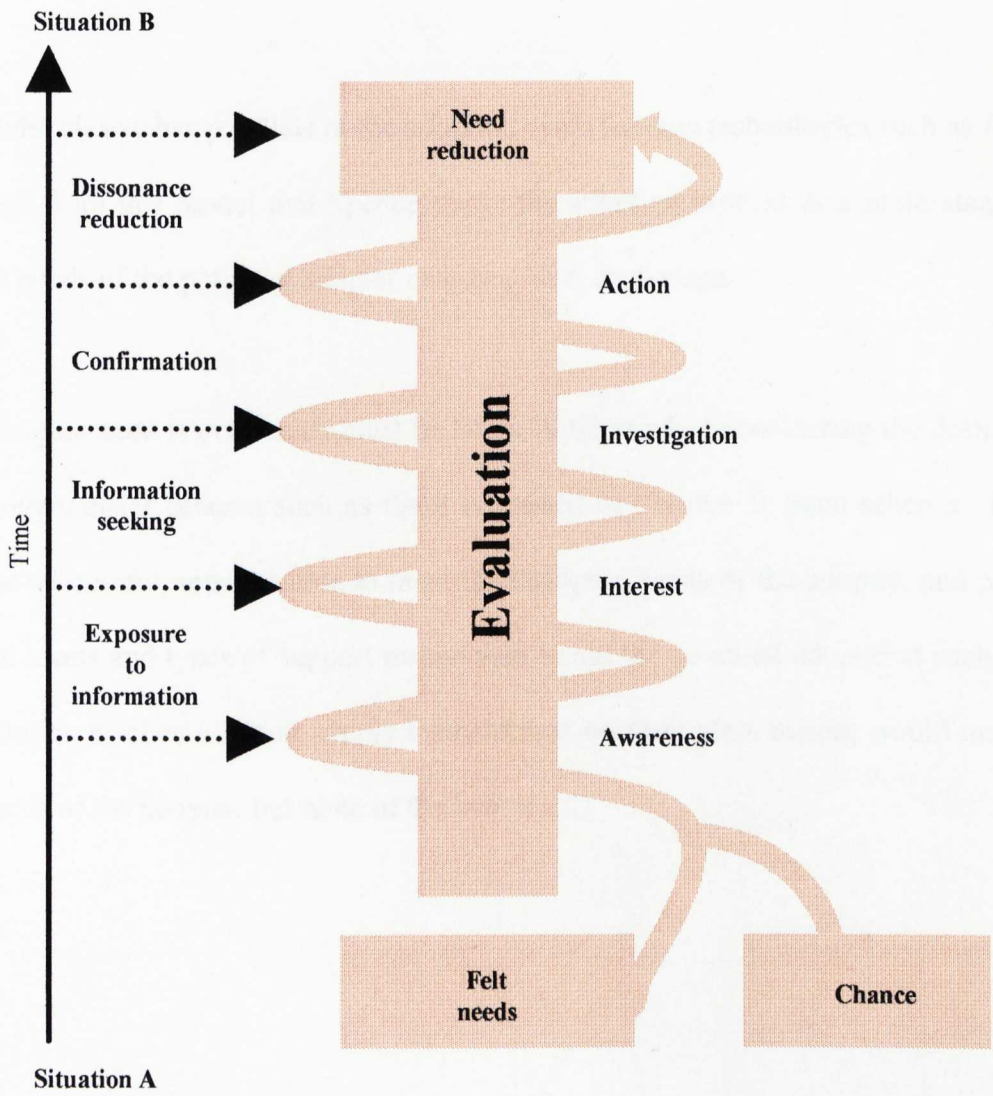


Figure 8-6. Adoption sequence

Spence considers that the adoption process begins with the emergence of a need in a user, either through a realisation of the need, or by a chance encounter. The adopter then passes

through a number of distinct stages (Awareness, Interest, Investigation and Action) before the initial need is satisfied or reduced. At each stage of this process, the adopter's requirements are different, and different approaches are needed to meet those changing requirements. These requirements change from the need for initial exposure to information in the early stages of the process through to final reduction in dissonance before adoption is complete.

This model clearly has parallels in the adoption cycle for new technologies such as ASICs. It is clear from this model that Spence views the adoption process as a multi-stage one, with the needs of the potential adopter changing with each stage.

This changing need is one which must be borne in mind when considering the design of a technology-transfer scheme such as those discussed in *Chapter 9*. Such schemes, if they are to be successful, must be able to meet the changing needs of the adopter, and provide different levels and types of support mechanism to aid the potential adopter at each stage. For example, a scheme which simply concentrated on awareness raising would meet the early needs of the adopter, but none of the later needs.

8.7 Collaboration and innovation.

One model which discusses the need for industrial collaboration in the innovation process is that produced by Rothwell and Zegveld (Rothwell & Zegveld,1985) and shown in Figure 8-7.

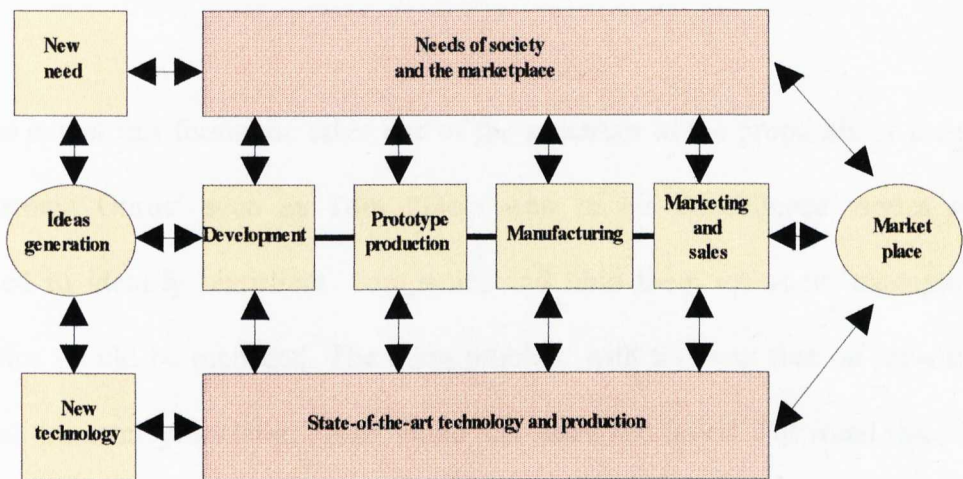


Figure 8-7. Collaboration and innovation

Rothwell and Zegveld regard the innovation process as being a sequential process that can be divided into a number of distinct stages from idea generation through to the marketing and sales effort necessary to turn an innovation into a successful product. They consider that the innovation process is dependent on a set of communication paths (shown as arrows in Figure 8-7) between the stages that can take place either within or outside an organisation. The innovation process itself is seen as the result of technological advances and market needs meeting in the innovative company. This model fits particularly well with the networked organisations discussed in Chapter 3, as the formation of communications paths between the core companies and the skills inherent in their suppliers is key in their success.

One problem with attempting to apply this model stems from its esoteric nature. For somebody attempting to be prescriptive in generating a solution to a specific problem rather than simply analytical, the model has no answers. It simply implies that putting the right sort of communications channels in place will eventually succeed, and assumes that say, excellence in manufacturing for your specific product is available somewhere. In some cases this may not be the case.

To some extent this forms the other end of the spectrum to the proposals of the so called 'management Gurus' such as Tom Peters who in his 'Excellence' series of books attempted to identify 'excellent' companies and hold them up as an example of how companies should be managed. The main problem with this was that on revisiting these organisations some years later, Peters found that some had failed. The trend since this time has been for academics to be far less prescriptive in their approaches, but this leaves those trying to apply management theory to real-life situations with a much harder task.

In terms of microelectronic adoption, this model also has some lessons for the designers of technology transfer programmes such as those discussed in *Chapter 9*. A technology transfer programme can be viewed as an enabling mechanism for the communication paths identified in the model. The role of such a programme would be to bring the innovative company into contact with those able to fulfill the roles which they cannot. This role could extend beyond initial technology, and into the manufacturing or marketing skills necessary to take a complete product to the marketplace.

8.8 Changes within an organisation

The models discussed earlier in this chapter relate mainly to the forces occurring around an organisation rather than to those occurring within it. The model discussed in this section relates more to the factors within an organisation that might advance or retard the adoption of a new technology.

Derek Pugh (Pugh, 1978) discusses four principals in relation to the acceptance of change within an organisation. Those principals are:-

1. **Organisations are organisms.** Pugh considers that organisations are not mechanisms that may be simply taken apart and reassembled in a new way. The implication is that changes in one area of an organisation must be considered in relation to the knock-on effects in other areas of the organisation.
2. **Organisations are occupational and political systems.** The implication here is that changes must be reviewed not only from the point of view of operational efficiency, but from the way in which they will affect ways of working, career prospects, and the power, status and prestige of those involved in the change.
3. **All members of an organisation operate simultaneously in all three systems (Resource-allocation, Occupational and Political).** This suggests that individuals will not be purely opposing or supporting a change from the point of view of one of the systems, and that opposition to a change may be more complex than simply a play for power or a move to career enhancement.

4. Change is more likely to be accepted by those basically successful in their tasks.

The suggestion here is that a change can be more readily accepted by a successful group who are simply experiencing some problem or difficulty than by those in unsuccessful groups who are likely to adopt a rigid approach in order to protect their position. The successful group is also likely to have confidence in its ability and a high degree of motivation to continue to be successful.

The implications of these principals for the adoption of microelectronics lie mainly in considering the likely reaction within an organisation when the new technology is introduced, perhaps by a small group, or in conjunction with a new and unfamiliar external organisation such as an external design-house.

Overcoming resistance within an organisation was discussed when identifying the role of the 'technology champion' in *Chapter 7*. The role of any technology transfer scheme can only be to provide the change agent with as much ammunition as possible in order to present logical arguments to the disparate groups within the organisation. The overcoming of political and other pressures encountered in introducing a new technology will be a major problem to be addressed by the individual organisation.

8.9 Conclusions from the adoption models.

The major conclusion to be drawn from these models is that the situation is not a 'black and white' one. While it is relatively simple to take each objection to adoption in isolation and show that the objection is unlikely to be based in fact, or only minor in direct consequence, the cumulative effect of all of these perceptions and facts on the overall system is a significant one.

The various models suggest a number of different approaches to increasing adoption, with different approaches being appropriate to different stages of the adoption process and to different people and groups involved in the process. As a result, it is unlikely that any short-sighted approach to a single problem will have more than a fleeting influence on the level of adoption.

Any route which aims to overcome objections and work towards greater adoption, whether originating in government, commerce, or both will need to be fundamental and long ranging in its approach if it is to have any chance of success. While short-term initiatives may spark the imagination of a few innovative companies, they cannot hope to increase adoption in the majority of organisations.

9. ASIC technology transfer schemes in the UK, Europe and the rest of the world.

The earlier parts of this study attempted to identify the reasons for non-adoption of ASIC technology and to identify models that might be used in order to more fully understand those reasons. The later parts of the study aim to use that understanding and the models identified in order to analyse how the situation might be improved, and to consider whether the attempts made by governments to increase adoption are likely to be successful.

Potential users of ASICs and the supply industry identified government intervention as one of the most important elements in increasing adoption. This chapter aims to review the level of intervention taking place in current UK and European initiatives and compare them with initiatives in operation in other parts of the world.

9.1 The UK: Microelectronics in Business.

9.1.1 Pre-history.

The Alvey programme, which started in 1983, represented probably the first major initiative funded by the UK government which encouraged participation in research between academic institutions and industry to the point of pre-competitive research and development. Faced with a situation where the UK was significantly behind its competitor nations (e.g. USA, Japan) in semiconductor technology the Alvey programme set out to close the gap, not by encouraging high-volume product development (e.g. semiconductor memory) but by encouraging the development of semi-custom technologies (cell and array-based technologies). To take any other approach would have been at odds with the strategy of the UK semiconductor manufacturers own strategies, and so unlikely to succeed (Hobday, 1990).

Most of the Alvey budget (£350M over five years) was aimed at projects in semiconductor process development. There was no post-competitive involvement, and none of the emphasis on the development of the capabilities of SMEs that was to become a focus of later initiatives. The focus of spending was very much in line with meeting the strategic niche objectives of the then UK semiconductor producers (GEC, Plessey, Ferranti and STC).

The Alvey programme can be considered to have been a success insofar as it encouraged the development of the base technologies necessary to support the increased adoption of microelectronics in UK businesses. It also sowed the seeds of industrial and academic cooperation that was to be important in later national and international initiatives. It did

nothing however to encourage adoption of the technology by end-user companies. This was identified as a problem in the late 80s (Hobday, 1990) and addressed in subsequent programmes. It can also be argued that in the longer term, the Alvey programme was not successful in helping to meet the strategic aims of the major UK semiconductor companies, as none of those identified (with the possible exception of the merged GEC-Plessey Semiconductors) have succeeded in becoming a world class manufacturer of semi-custom devices.

A number of small initiatives had been organised by the DTI in support of microelectronics adoption in the UK (e.g. Custom Silicon Now). But, in the late 80s surveys continued to show that adoption of the technology was still slow. One major survey of this type was that performed by Shortland Associates (Shortland, 1991) and discussed in *Chapter 4*. Government initiatives had traditionally focused on dissemination of information via seminars, and some very limited financial support to industry and academia (e.g. for the purchase of CAD equipment under the ECAD scheme). While sufficient to act as a catalyst for entrepreneurial companies, these schemes were not far-reaching enough to convince the majority of potential users to adopt ASIC technology. The market for ASIC technology among electronics companies was reaching the 'early adopters' stage (see *Chapter 6*), so the level of intervention required to induce adoption was far greater than the government initiatives were providing. The supply industry was also unable to provide sufficient support for the reasons discussed in *Chapter 6*. In essence, the cost of marketing to potential users was not economic when compared with the level of business that they represented. In consequence, a market-failure existed.

Industry began to push the DTI for some initiative in this area. For example, the author gained DTI support for a regional seminar on ASIC technology in 1992 (McArdle and Woodley, 1992). This small-scale seminar and exhibition (50 delegates) was successful, not only in its initial intent, but in helping to catalyse the DTI into adopting a similar set of events, though on a much larger scale, to act as the promotional front to 'Microelectronics in Business'

Following some years of planning, Microelectronics in Business (MiB) was launched to address the market failure identified above. Its first promotional seminar took place in Manchester in April 1994.

9.1.2 The Microelectronics in Business technology transfer model.

The model for technology transfer adopted by MiB was a relatively simple one, and is shown graphically in *Figure 9-1*.

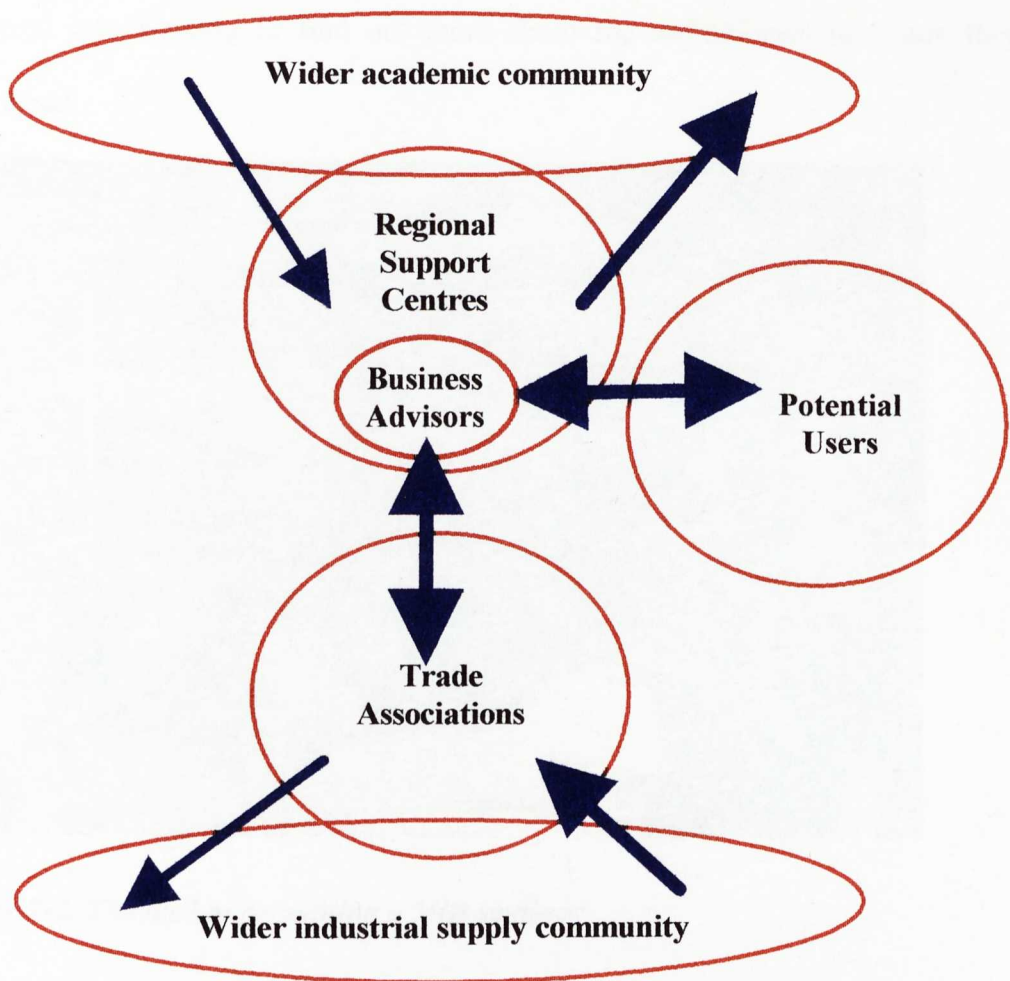


Figure 9-1 The Microelectronics in Business Programme.

Following initial promotional activity (e.g. by mail-shot), the 'Custom Circuits Seminar' and later the 'Think Digital! Seminar', acted as a front-end to the programme. The seminar (Figure 9-2) provided initial contact with potential users, an introduction to ASIC technology, and a number of case studies showing how some UK companies had been successful using ASIC technology in their products. This approach can be easily put into a marketing context. Adopters from the 'early majority' stage onward can be shown to react positively to suggestions that the path they are about to follow has been successfully followed by their peers, while the entrepreneurs in some market segments could be

catalyzed into wanting to find out more about the technologies to which they were introduced.



Figure 9-2. The author presenting a MiB seminar

Following the seminar, potential users were introduced to a DTI Support Centre. The DTI established first two, and later a total of six regional support centres based at higher education establishments (see *Figure 9-3*). These centres were equipped with suitable design tools and support staff, and were intended to act as learning centres where users could learn to use the tools and the technology as well as gaining independent advice on the adoption route most appropriate to them. Solutions were available in a number of technologies from FPGA through gate-array to standard-cell.

Each centre also each appointed a 'Business Advisor', with considerable industrial experience, who could guide potential users through the business decisions inherent in the adoption of the new technology, and could if necessary suggest how the user might

interface with the supply industry should they need the help of commercial designers or ASIC supply companies.

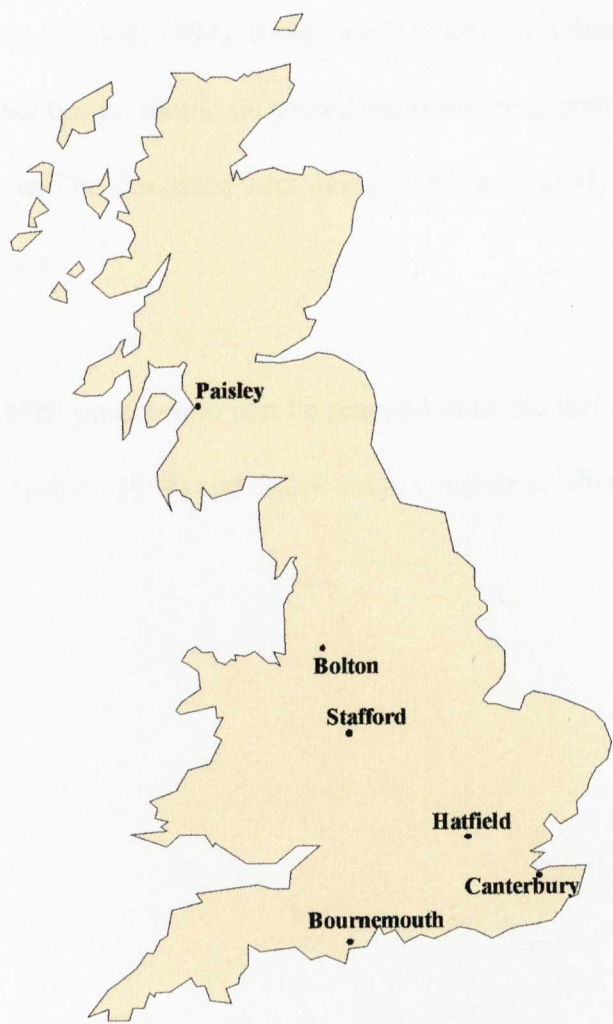


Figure 9-3. MiB Regional Support Centres.

Region	Location	Institution
South West	Bournemouth	University of Bournemouth
Kent	Canterbury	University of Kent
South East	Hatfield	University of Herts
North	Bolton	Bolton Institute
Scotland	Paisley	Robert Gordon Institute
Midlands	Stafford	University of Stafford

Table 9-1 MiB support centre locations

It was not the intention of the DTI that these centres should become sub-contract design centres. Indeed, considerable pressure was put on the DTI by the supply industry to ensure that this did not happen (Merritt, 1994). It was the DTI intention that projects identified as suitable for sub-contract design should be passed out from the support centres to the design industry. However, as will be discussed later, this proved particularly difficult to achieve in a visibly unbiased manner.

The approach of the MiB programme can be mapped onto the technology transfer model proposed by Spence (Spence, 1994) and discussed in *Chapter 8*. This is shown in *Figure 9-4*.

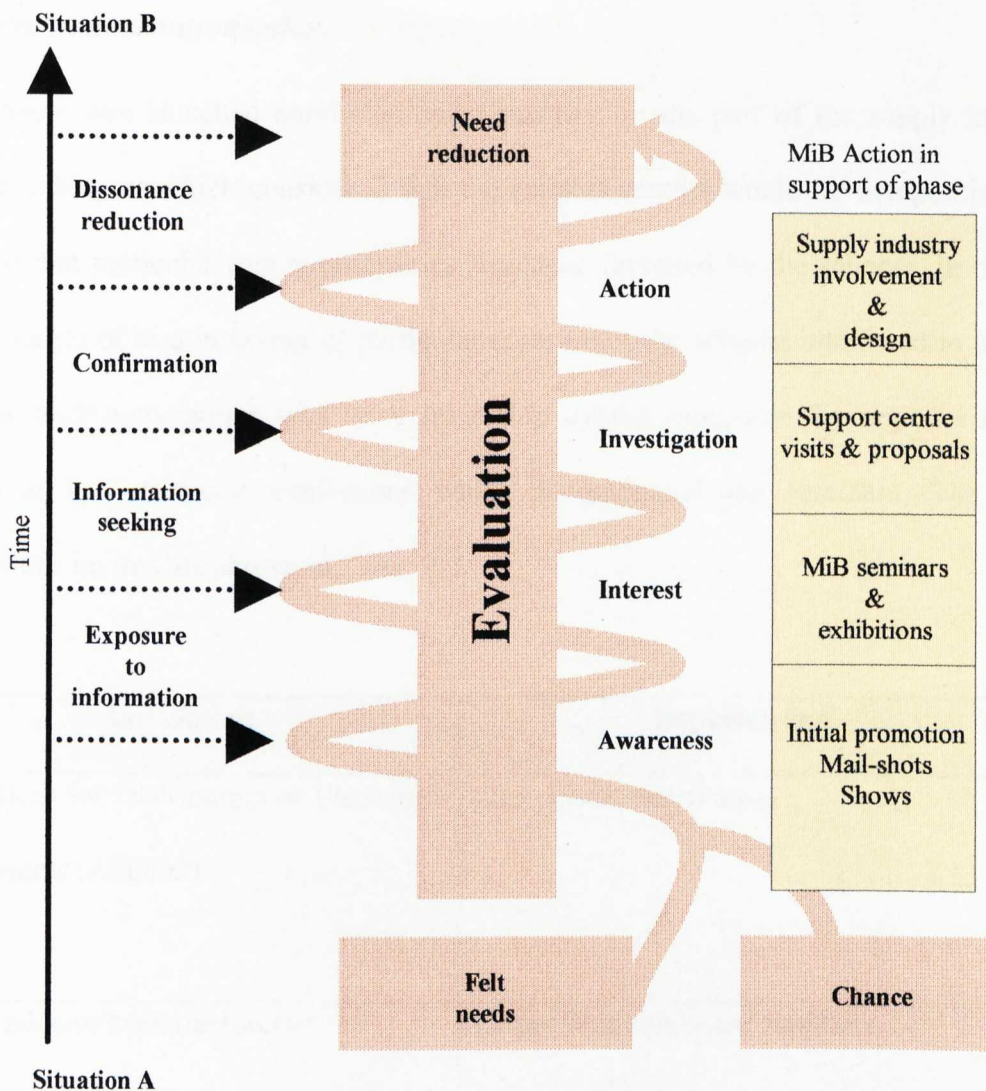


Figure 9-4. MiB related to the Spence adoption model

The four stages of the evaluation process identified by Spence were supported by different elements of the MiB programme. Initial awareness was addressed by mail-outs to potential users, and by the sponsoring of stands at suitable trade exhibitions. When adopters entered the 'interest' phase, they were invited to attend a seminar, and the subsequent 'investigation' and 'action' phases were supported through the activity of the regional support centres, who were able to provide very specific support targeted to individual companies, and also to help those companies to find suitable industrial suppliers.

9.1.3 Programme introduction.

The scheme was launched amid significant mistrust on the part of the supply industry, some members of which considered that the support centres would be competitive with them, or that particular supply-companies would be favoured by the scheme. In order to avoid charges of bias in favour of particular companies, the scheme interfaced to industry via four trade-associations who were invited to exhibit alongside the regional support centres at the afternoon exhibitions which accompanied the seminars. The trade-associations invited are shown in *Table 9-2*.

Association	Representing
Association for Distributors of Electronic Components (AFDEC)	Component distributors
Semiconductor Manufacturers Association (SMA)	Larger semiconductor suppliers.
Semiconductor Businesses Association (SBA)	Mainly design houses and some EDA companies.
VHDL UK	User group of advanced EDA tools.

Table 9-2. Trade associations active within MiB.

9.1.4 Early mistrust.

The early response of the supply industry was not all positive. The establishment of the support centres at HEIs was not a popular decision within industry, who claimed that such institutions would not be able to provide industrial quality services, particularly with respect to high-volume design and manufacture. The design houses were concerned that the HEIs would in some way become industrial design centres in competition with them, and subsidised by the DTI. This real concern grew as, some months after the beginning of the programme, the industry had not seen any of the promised new clients.

This distrust became evident in the UK electronics press in the latter part of 1994 (Flaherty, 1994. Wilson, 1994). However, the truth of the matter was that the support centres were simply becoming overloaded with clients who in the main did not want design support of the complexity offered by design houses as their applications were of a type that could easily be supported through FPGA solutions that they could design for themselves. The major semiconductor companies also began to become disillusioned with the scheme, because they were not meeting any significant opportunities while they were spending money sending staff to the seminar related displays. At one stage it looked as though SMA might withdraw its support. (Whittaker, 1994)

9.1.5 The first design.

The feeling of mistrust of the HEIs was not helped when the press release of the first completed design to pass through the programme was made in March 1995 (Joselyn, 1995). The design had been a relatively simple FPGA based product, but when design assistance was requested, the client had been passed to a design support group within the

HEI at which the support centre was located rather than out to industry (Wilson, 1995:2). It later became obvious that this had been a correct decision, but its lack of transparency did not help the design industry to accept that a correct route had been followed.

9.1.6 Building industrial links.

It quickly became apparent to the DTI that the support of the supply industry would be crucial to the success of the scheme. The level of support and third-party design required by some of the companies approaching the support centres was beyond what could be realistically provided under the scheme. However, it was important that the DTI was seen to be impartial. The support centres could not be seen to be biased toward a particular design house. But, companies were asking, 'Where can I get my design done?'. It is at this point that the role of the trade associations started to emerge as important in the technology transfer process.

A method of recommendation was developed between the DTI business advisors and the Semiconductor Businesses Association (SBA). Potential users of design services were introduced to an assessment panel within the SBA who would then suggest a number of potential suppliers. In this way, the impartiality of the support centres could be maintained, and some level of pre-selection of suppliers achieved which would be more likely to result in a successful project than having the user pick a design company without any help.

9.1.7 Results of the first year.

The sales process for ASIC designs is long, with a year or more being typical. In August 1995, over a year after the start of the scheme, a press release from the DTI claimed some 18 design starts in various technologies (Wilson, 1995:1). Four SBA members (Array Consultants, Plextek, Swindon Silicon Systems and Elex) publicised the fact that they had received orders from clients introduced through the MiB initiative.

It is difficult to ascertain the full impact of the MiB programme in its early stages, but some indications can be drawn from the results of a telephone survey conducted by Plextek Ltd between June and October 1995 (McArdle and Ireland, 1996). Plextek attempted to contact all of the companies that had attended the first round of seminars. Taking the database of MiB seminar attendees as a starting point, the survey attempted to contact one representative of each attending company. When the database was reduced to eliminate non-industrial seminar delegates and multiple attendees from a single company, the result was a list of 346 'relevant' companies. The sample is statistically large enough to draw some interesting indications from the results.

The phase of adoption of the 346 companies who were considered 'relevant' at the time of the survey is shown in *Figure 9-5*.

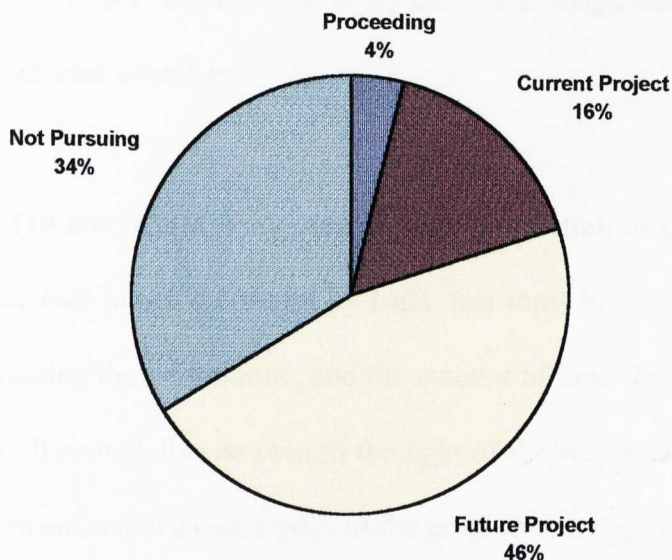


Figure 9-5 Adoption status of contacted companies

In total, around two-thirds (66%) of the relevant companies were either engaged in the use of technologies covered by Microelectronics in Business or were considering their use for a current or future product development. This represented some 214 different companies, and should be viewed as a success for the programme.

The applications ranged over a wide variety of markets, from simple domestic appliances to a novel drug-delivery system. The participating companies also varied widely, from small start-ups to established SMEs.

Clearly the scheme was having a positive effect. The supply industry, seeing real business being generated became far more supportive of the initiative. At an SBA committee meeting held in the summer of 1995, a show of hands indicated that most of the fifteen companies present had seen some business generated directly as a result of MiB, and the

survey detailed above revealed that some non-SBA design consultancies had also started designs for seminar attendees.

While 4% (14 companies) may seem a small proportion of companies to have begun a design in the technologies covered by MiB, this must be seen in relation to the type of company entering the programme, and the amount of time for which they had been in the programme. It should also be seen in the light of the very small market for ASIC designs by SME companies that existed prior to the programme. Figures derived from the supplier survey performed for this study suggest that around 20 masked-ASIC design starts can be attributed to SMEs each year along with an unknown number of design starts in other microelectronic technologies.

These results also represented an increase in adoption over the rates found by surveys performed prior to the MiB programme, although the technologies forming the basis of those surveys are slightly different from those covered by the present MiB programme (Shortland, 1991).

9.1.8 Types of companies involved in the programme.

The distribution of companies shown in *Figure 9-5* can be mapped fairly closely onto the adopter classifications suggested by a number of researchers who discuss the rate of technology adoption by companies and individuals (Spence, 1994. McArdle, 1996:1. McArdle, 1996:2). This adoption cycle is shown in *Figure 9-6*, and discussed more fully in *Chapter 6*.

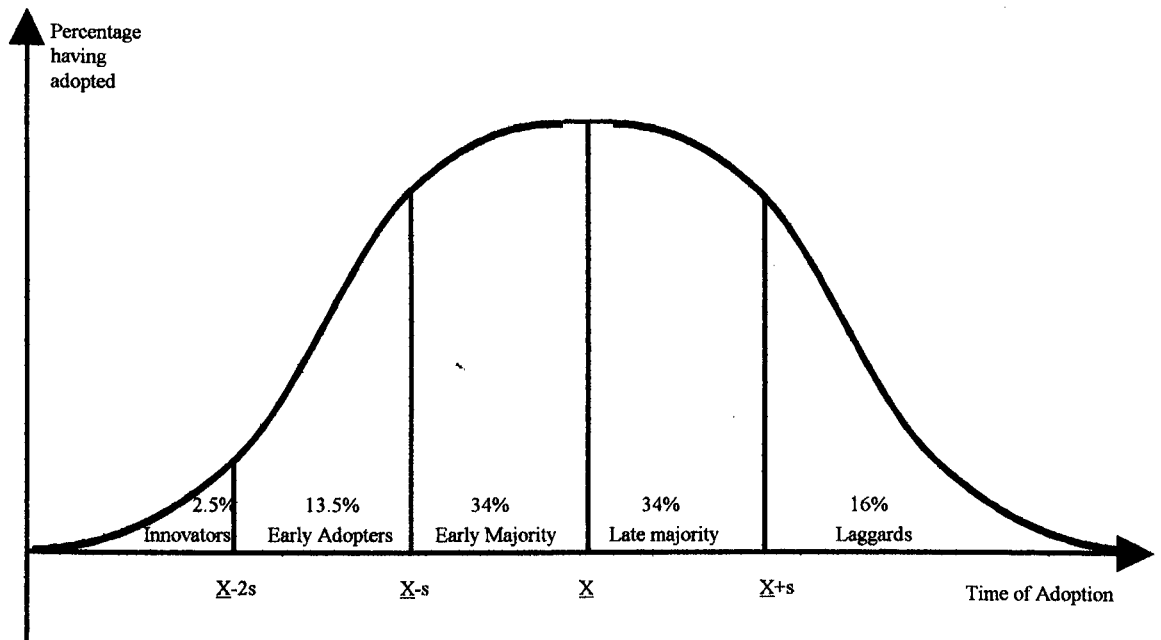


Figure 9-6 The adoption cycle

If one makes the assumption that the few companies who have started microelectronic projects fall into the 'Innovator' stage or the early phase of the 'Early Majority' phase, then it follows that the vast majority of companies encountered fall into categories other than 'Innovator'. This has a number of implications on the way in which these companies should be treated if adoption is to be encouraged.

Only 'innovators' will move forward at their own initiative. Members of the other groups are known to require much more pro-active encouragement if they are to become adopters. Classically such encouragement would include:

- Peer pressure - Knowledge that other companies have adopted the technology and may be using it to compete against them.

- Acceptance - Knowledge that other companies have successfully adopted the technology without falling into any of the pits that they themselves fear.

As noted earlier, it is often the case that the early majority will act as legitimators to the later groups, even more so than innovators who are often perceived as excessive risk takers. The late majority companies are likely to be extremely ponderous in their approach, and laggards are often openly hostile to change, and may currently be saying 'No' when asked if they intend to adopt microelectronic technology.

9.1.9 Timing of companies in the adoption cycle

Some interesting trends can be ascertained regarding the timing of adoption of these technologies. Using information supplied by one design-house that was successful in securing design business from companies introduced by MiB, it is possible to calculate the time taken from the point that a client attended a seminar to the time that they requested a proposal for design work, or following that proposal placed an order for design work.

Data regarding proposals are statistically more significant than those regarding sales, as at the time of analysis proposals existed in much larger numbers than final sales. The distribution of seminar to proposal times is shown in *Figure 9-7*.

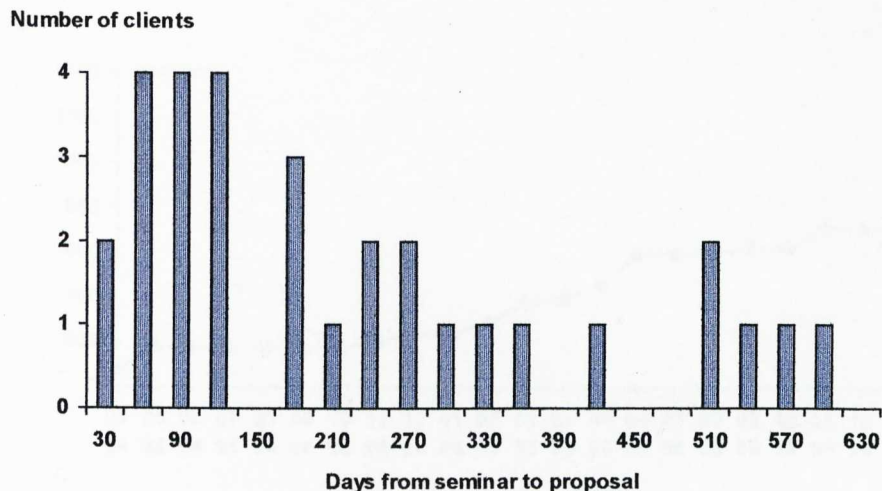


Figure 9-7 Time from seminar to proposal

It can be seen from *Figure 9-7*, that although some entrepreneurial companies do proceed straight from seminar to proposal in a relatively short time, the majority do not. In fact, the average time from seminar to proposal is over seven months (213 days). It must however be remembered that this is the time to proposal. The time to order is significantly longer. Although not yet statistically significant, the average time from seminar to order was well over a year at the time of analysis. These timings are considered to be fairly typical of 'new name' clients by the supply industry, and not specific to MiB related contacts.

9.1.10 Rate of entry to MiB

The rate of entry of new clients to the MiB programme is shown in *Figure 9-8*.

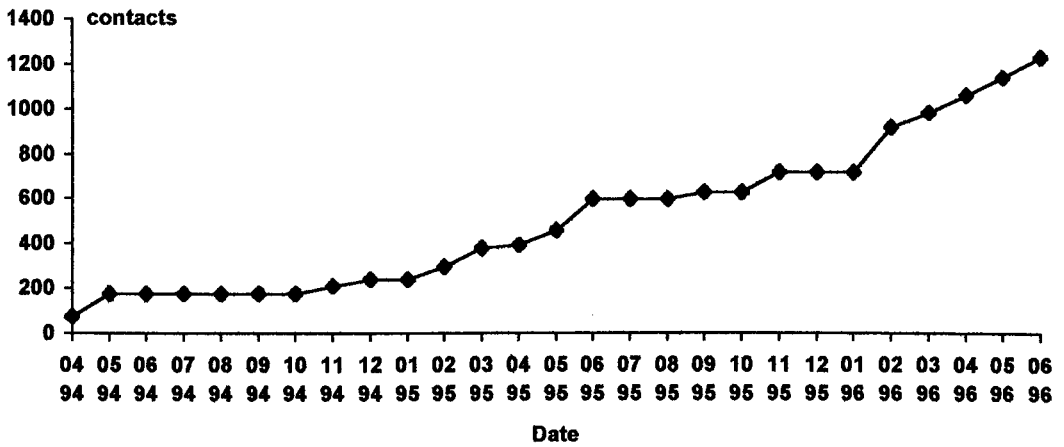


Figure 9-8 Total contacts in MiB programme (seminar delegates)

Contacts up to November 1994 are those generated by the pilot series of the Custom Circuits Seminar, so may to some extent be discounted because support centres were at an early stage of developments, and links to industry were still being established.

The main phase of the programme began in November 1994, and the number of companies entering the programme rose steadily thereafter. It began to rise steeply in early 1996 as the Think Digital! Seminar series began. This series, which was free of charge (Custom Circuits had a £50 seminar fee) attracted a higher number of seminar delegates, although interestingly, these seminars also had a higher proportion of pre-booked attendees failing to show at the seminar. Perhaps free seminars are viewed as having less value than those for which a charge is made.

9.1.11 Industrial categories in which contact companies operate.

The classification of the contacts in relevant companies within the MiB programme at the time of the Plextek survey is shown in *Table 9-3*.

Industrial Categorisation	qty	%
Unknown	127	37%
Instrumentation	72	21%
Control Systems	29	8%
General Electronics	17	5%
Telecomms	17	5%
Process Machinery	13	4%
Security	13	4%
Medical Products	11	3%
Computer Equipment	9	3%
Components	8	2%
Domestic Products	8	2%
Vehicular	5	1%
Professional Audio	4	1%
Heavy Engineering	4	1%
Acoustic	2	1%
Aviation	2	1%
Broadcast Equipment	2	1%
Food Industry	2	1%
Leisure Products	1	0%

Table 9-3. Industrial categories of contacts

The companies have also been split into broader industrial categories. The result of this categorisation is shown in *Figure 9-9*.

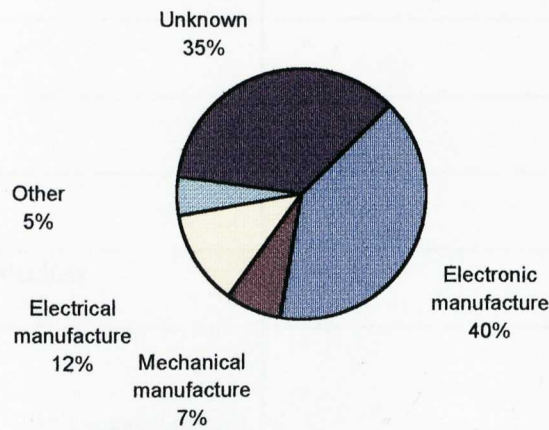


Figure 9-9 Broad industrial classification of contacts

As might have been expected, the majority of companies were involved in electronic products, but a significant proportion came from non-electronic based companies where the proposed technologies could bring significant product and competitive advantage.

9.1.12 Later results of MiB

Further telephone surveys were not performed in later stages of the programme, but figures available from the DTI summarising the overall results for the MiB programme up to September 1996 are shown in *Table 9-4*. (DTI, 1996:1).

Promotion contacts (e.g. by mailshot)	129,000
Initial inquires	2,835
Seminar delegates	1,209
Live enquiries	1,649
Completed feasibility studies	267
Project starts	
At support centre	35
Client designing	23
Passed to supply industry	36
Completed projects	14

Table 9-4. MiB results to September 1996

It is interesting that the ratios that can be derived from these figures are similar to those identified by the supply industry as expected returns from marketing activities (see *Chapter 6*). MiB achieves a ratio of approximately 100:1 for mail-out to seminar attendee compared with around 100:1 mail-out to initial meeting (arguably requiring a higher level of commitment) claimed by the supply industry.

The mix of technologies resulting from feasibility studies also gives an interesting view of the most appropriate technologies for new users of ASICs. The split of proposed technologies is shown in *Figure 9-10*.

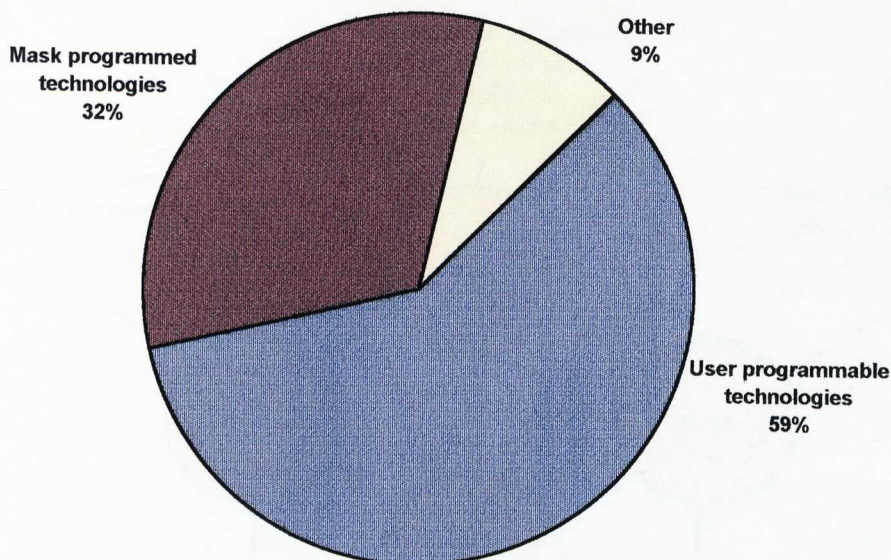


Figure 9-10. Technology split among MiB clients.

It can be seen from this that although mask programmed technologies do have a significant role to play, by far the majority of new users coming into the MiB scheme have applications which are best served by user-programmable technologies such as FPGAs and microcontrollers.

9.1.13 Reasons for the success of MiB

Although not endowed with a particularly large budget (some £4 million) MiB was, and continues to be, a successful programme. Some of the reasons for this can be suggested from the Spence model discussing ‘factors relating to innovation’ discussed in *Chapter 8*. That model suggests Cost, Complexity, Visibility, Divisibility, Compatibility, Utility and Collective action as the major factors in the acceptance of new technology. This model, in relation to MiB, is shown in *Figure 9-11*.

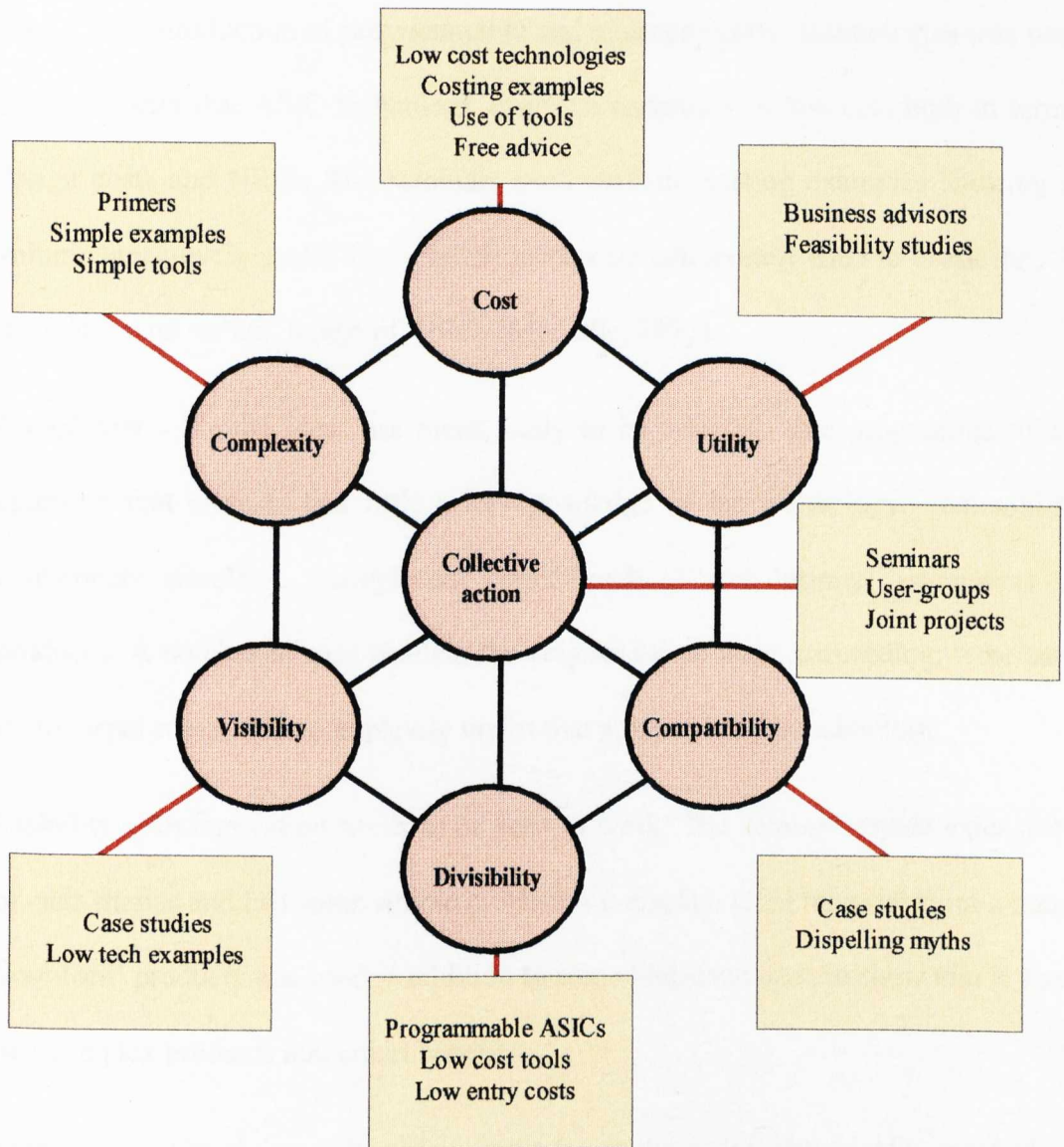


Figure 9-11. MiB related to Spence's adoption factors

Before taking these factors individually, it is important to consider that MiB made a significant change in the definition of ASIC as a technology by considering that all of the ASIC technologies defined in this study, ranging from masked ASIC through programmable ASIC to microcontrollers could all be described as ASIC. Having established this definition, a new message could be brought to potential users in the following way:

- **Cost** - The introduction of programmable and microcontroller technologies was used to show adopters that ASIC technology could be realised at a low cost both in terms of design costs and NREs. The seminars used realistic costing examples showing low-volume break-even levels. The seminar presenters deliberately tried to break the, 'Real men do it with masks' image of ASICs (McArdle, 1995).
- **Complexity** - Simple ideas are more likely to be adopted. The programme took the approach that entrants had little prior knowledge of the technology. Seminars were deliberately simplistic (though not condescending) and 'primer' documents were produced. A number of case studies, showing first-time users succeeding, were used to try to dispel some of the complexity myths that surrounded the technology.
- **Visibility** - An innovation needs to be seen to work. The seminars made extensive use of case studies and had some simple products on display. Case material from a range of 'low-tech' products was used in addition to some high-tech ones to show that it was not just complex products that could benefit.
- **Divisibility** - The ability to be able to put a toe in the water. Historically, masked ASIC were an 'all or nothing' technology requiring large investments and significant commitment before any reward was evident. By emphasising the role of programmable technologies, the programme was able to give companies the opportunity of low-cost trial designs which would get them onto the ASIC ladder. Use of the design tools at the support centres made the necessary level of commitment even lower and so far more easily justified.
- **Compatibility** - It was necessary for the programme to try to dispel some outdated horror stories while still being realistic about the risks that still remain with more advanced technologies. Case study material was used extensively to achieve this.

- Utility - The ability of a technology to have an immediate use was addressed on a case-by-case basis by having business advisors and support centres perform feasibility studies relevant to the product needs of individual companies. The immediate benefits of the technology to the clients own products could then be demonstrated
- Collective action - The bringing together of a group of people at seminars, and the repeated use of successful case studies was key in adding peer pressure to the persuasion methods used on prospective adopters. Other collective action included the establishment of user-groups at support centres, and the encouragement of joint projects where non-competing companies could be brought together.

So in terms of the factors identified by Spence, the MiB programme brought together a powerful mix of positive factors that had not previously been brought to bear on the target participants.

MiB can also be considered in a positive light when compared to the idealised model proposed by Rothwell and Zegveld (see *Chapter 8*). They see the innovation process as being a set of sequential steps which are facilitated by the development of formal and informal communications networks and channels between innovative companies and agencies that have knowledge of, or access to, the technology that they need to adopt. Rothwell (Rothwell,1994) suggests that this process has evolved from the 'technology push' and 'market pull' models that were assumed in the 1950s and 60s. He claims therefore that the process is less deterministic than had been previously assumed.

This would suggest that a technology transfer scheme requires a multi-faceted approach which encourages formal and informal linkages to be made. The MiB approach supports

the establishment of such linkages at a number of levels. Innovative companies are encouraged to meet others at seminars, support centres and exhibitions. They are given access to both academic and industrial collaborators through introductions by Business Advisors, and can make contacts with 'best-in-class' suppliers at all stages of the adoption process from initial conception of a new product through to the manufacture and marketing of the finished product through links to industry trade associations.

9.1.14 Conclusions on the Microelectronics in Business programme.

A number of the conclusions reached in this analysis can be considered to have direct relevance to the existing and continued activities of the Microelectronics in Business programme. They include:

- Microelectronics in Business has made a significant impact on the adoption of ASIC technologies by the UK manufacturing base. The number of design starts already achieved is significant (McArdle, 1996:3) and the indications are that the majority of design starts are yet to come.
- The long time-scales between introduction and adoption suggests that most of the design starts that will be generated by the programme will come over a year from the point at which a user enters the programme. As the typical client is of a category other than 'innovator', it is likely that the interest in the technology will wane if it is not supported by continued exposure, example and reassurance. The indication is that the work of the support centres should be seen as a long-term activity (perhaps 4-5 years) rather than a short term one. The support activity will need to operate for some time after new entrants stop coming into the programme.
- The ability of the support centres to cope with the number of clients being introduced to them is seen as a limiting factor by some clients. This might suggest that increased activity is required, at least at the early stages of contact. From a DTI point of view this should involve competent, impartial business and technology advice irrespective of whether that is to be followed with the technical involvement of a university based support centre or a commercial design service.

- The continual exposure of potential users to a 'technology rich environment' is important if adoption is to be encouraged in the less dynamic organisations. A number of areas that might be used as vehicles for this exposure were identified both in the telephone survey, and from seminar delegates. The major two were:
 - Formal design methods
 - EMC issues

Both of these areas could be considered for further seminar, publication or video activity.

- From an industrial point of view, the potential clients being introduced by the programme are ones that design companies and suppliers would not normally encounter. Given limited marketing budgets, design houses will naturally concentrate on larger companies where their chances of success are higher (This is discussed in *Chapter 6*). The initial awareness raising and introduction provided by the MiB programme would not be performed naturally by industry. In consequence, the likely result of an end to the MiB programme would be that smaller companies would once again be ignored, and so the spiral of ignorance, misinformation and non-adoption would return.
- The European initiatives aimed at first users (e.g. Europractice and FUSE) are complimentary to the MiB programme in providing funding for a small number of companies to implement their products, but do not address the wider areas of awareness raising and initial introduction performed by MiB. Without the initial activities it is possible that FUSE would result in a few companies who are

experienced at grant application being successful, rather than a more general increase in awareness and adoption of ASIC technologies.

9.2 Europe: **EUROPRACTICE.**

Shortly after the start of the main phase of Microelectronics in Business, the European Commission launched the Fourth Framework. This is a multi-billion ECU scheme covering all of the EU investment in research and development. Of interest to this study is Europractice, and particularly the First User Action (FUSE) scheme. This is a scheme aimed at increasing the uptake of microelectronics and replacing the Eurochip and ChipShop initiatives. The structure of the scheme is not dissimilar to that of MiB, but the degree of funding (20M ECU over four years) meant that the degree of direct intervention could potentially be greater (Anon, 1995:1). The basic structure of Europractice is shown in *Figure 9-12*.

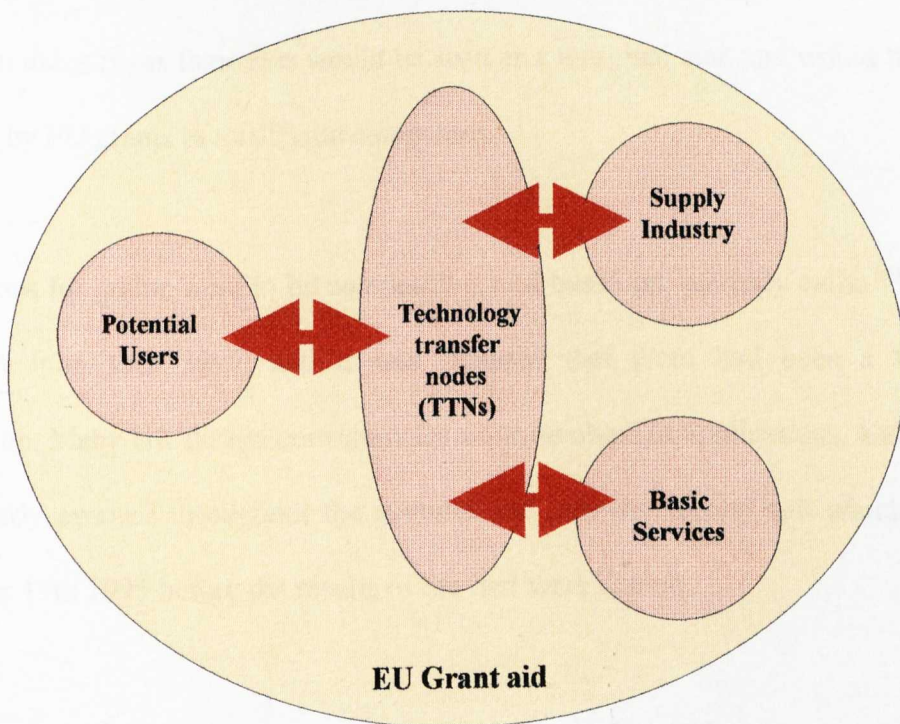


Figure 9-12 *The structure of Europractice.*

The EU funded the establishment of a number of 'basic services', such as a multi-project wafer service and semiconductor testing services, which could be called upon at subsidised rates by users. In order to catalyze the technology transfer process, twenty Technology Transfer Nodes (TTNs) were set up across Europe. In the UK, these were mainly located at the MiB support centres mentioned earlier. In addition to this infrastructure, the EU directly subsidised the cost of the adoption of new technology by grant-aid under the 'First User Action' (FUSE) scheme.

Under the FUSE scheme, users making first use of a microelectronic technology such as ASICs could apply for 100% funding of marginal costs involved in adopting the technology for a specific product. It was assumed that some companies would need to use external agencies to perform the design. Clearly this was seen as a positive approach by the UK design industry, as their fees would be seen as a marginal cost and would therefore be fully paid by EU grants to qualifying companies.

Applications for grants were to be competitive, and based on quarterly calls. The first call closed on June 15th 1995, and it was reported that there had been a large over-subscription. Many UK design consultancies were involved in applications, and the results were eagerly awaited throughout the summer and past the second call which closed on September 15th 1995 before the results of the first were known.

However, there was some unease in the design industry during that summer. By invitation of the DTI, a representative of the EU department assessing the grant applications addressed the UK design industry in June 1995 and disclosed some of the criteria under which applications were being judged. It became apparent that companies who wished to

perform design of ASICs internally were being given priority over those using third-party design. There was an immediate response from the delegates at the meeting, who claimed:-

- Third part design was the most valid business model for many SMEs
- Internal design of all but the simplest ASIC was more likely to end in failure
- Direct intervention on that scale would unbalance a delicate market

There was a clear feeling that badly placed intervention which rewarded companies doing internal design over those who used third-party design could be disastrous to the UK design industry.

9.2.1 Results of the first calls.

The results of the first award review were announced in October 1995, some 4 months after the closing date for applications. Actual grants were not to be awarded until mid 1996 following protracted negotiation between the EU and grant winners. The results of the next two calls were also late in being published because the EU had badly underestimated the high level of response to the calls. The results of the first three calls are shown in *Figure 9-13* (Eglin & Bloemendaal, 1996).

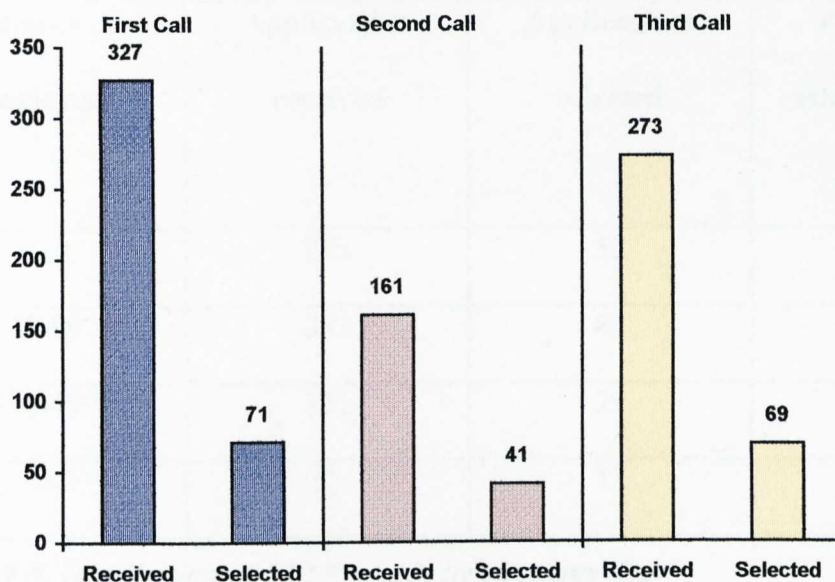


Figure 9-13. FUSE. Results of first three calls.

UK companies were particularly successful in gaining approval, with 9 of the 71 selected projects in the first round being UK in origin. This success was put down, at least in part, to the support in preparing proposals that had been provided to companies under the Microelectronics in Business programme. Applicants were able to produce costed proposals in association with the MiB support centres, and incorporate the information directly into their FUSE applications. Over the first three calls some 58 of the 181 selected projects were from UK companies.

Although not exclusively aimed at SMEs, some 93% of proposals came from the SME base (using the European definition - companies of fewer than 500 employees). In addition, 93% of selected projects were also SME based. The precise distribution of company size is shown in *Table 9-5*. It should be noted that the figures given in *Table 9-5*, although from the same source, differ slightly in total from those shown in *Figure 9-13*. The reason for this is unknown.

Number of employees	Applications received	Applications selected	Percentage selected in this category
<10	245	52	21%
10-99	333	83	25%
100-499	121	29	24%
>499	53	13	24%

Table 9-5. Distribution of FUSE grants by company size.

So in this respect, the FUSE programme could be shown to be supporting the SME base, and the number of grants awarded to UK companies suggested that the programme was also a success for the UK.

The technologies involved in the proposed and successful projects are shown in *Figure 9-*

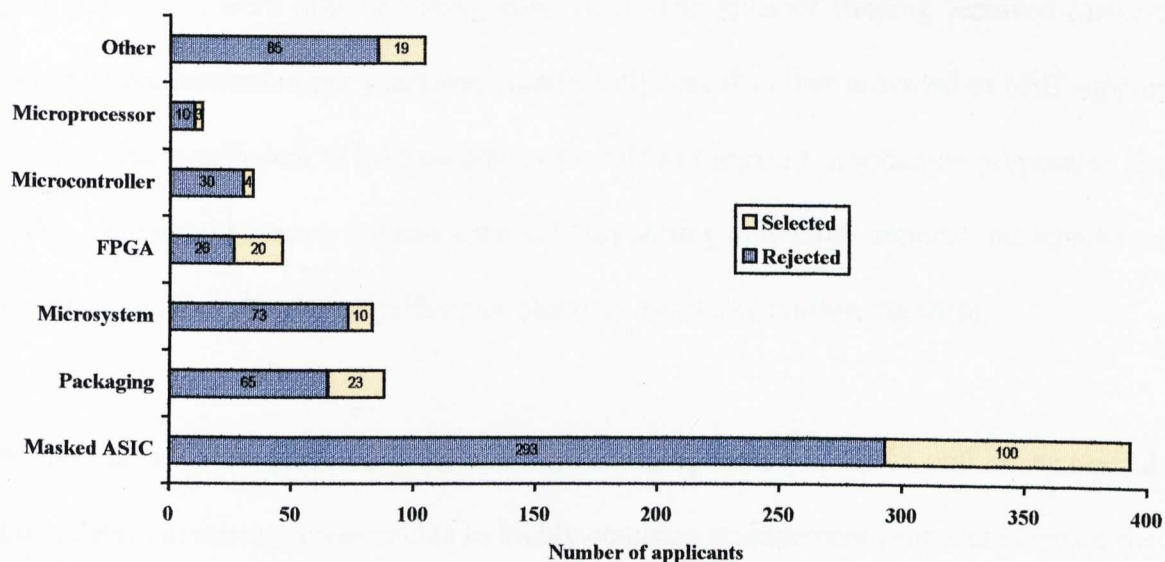


Figure 9-14. FUSE. Technology spread addressed

It would appear from these results that although masked ASIC generated most proposals, only 25% of them were successful. Companies proposing FPGA projects were more likely to succeed (43% success rate). It must be assumed that this is due to the project assessors judging this the most appropriate technologies for the ‘first users’ who applied. This is very much in keeping with the results of MiB. However, there did seem to be some evidence of massaging of figures to meet quotas. Some of the projects receiving funding for masked ASIC development were clearly uneconomic (e.g. full mixed signal devices in low added-value products with volumes of a few hundred per year).

It also became apparent at this stage that some of the fears of the design industry had been justified. The assessors of potential projects had been given clear guidelines on acceptable projects, and had applied these guidelines strictly. Specifically, sub-contracting more than 65% of the total grant led to disqualification, meaning that once manufacturers’ NREs had been paid, there was little left for sub-contract design work.

The new TTNs were also becoming concerned. The level of funding received (around 50kECU per institution per year) was significantly less than that provided to MiB support centres, and insufficient to take on any extra staff to prepare Europractice proposals. The TTNs were to take a more ruthless approach, supporting only those applications which met the Europractice (unwritten) guidelines, and thus inevitably reinforcing them.

At the time of writing, it is unclear whether the Europractice initiative will be successful. Long delays in starting projects due to highly complex management procedures meant that few finished projects were being publicised in early 1997. Indeed, some companies that had been successful in obtaining early approval later abandoned projects as delays in receiving grants increased. Other companies found that they were being encouraged to use technologies that were no longer appropriate to their product needs due to the emergence of new, more suitable devices than those which had been approved in grant applications.

9.2.2 Relating Europractice to the adoption models.

In terms of the adoption models identified in *Chapter 8* and applied to MiB in this chapter (*Figure 9-4 and 9-11*), Europractice cannot be considered to be a complete technology transfer programme. It certainly addresses some phases of the adoption process to a high degree by direct financial support of the later stages of adoption (the 'action' stage), but it does little to support the earlier 'awareness', 'interest' or 'investigation' stages (McArdle, 1996:3).

It may be that some companies have found themselves skipping some of the earlier, and very important, stages of the adoption process due to the lure of available grant-aid, only to

find that they lack the commitment to carry the project through when problems appear during implementation. It is also possible that in making the jump directly to implementation, the companies have not had sufficient time to build the network of communications channels and support systems implicit in the Rothwell & Zegveld model (*Figure 8-7*) and so have nowhere to turn when implementation becomes difficult.

9.3 Other schemes operating in the UK.

Although the two schemes discussed above are, at the time of writing, the most active in direct intervention in ASIC adoption, a number of other schemes and sources of development finance exist both in the UK and overseas. Such schemes are generally not restricted to ASIC technologies.

9.3.1 Support for Products Under Research (SPUR)

This scheme helps UK businesses with less than 250 employees by providing a grant of up to 50% of the costs of new product or process development. The scheme is a competitive one, and the maximum available grant is £150,000. Successful applications are expected to show a high degree of technical innovation in addition to commercial viability.

9.3.2 Small firms merit award for research and technology (SMART)

This UK based scheme is only open to companies of fewer than 50 employees. It is an annual competition with a maximum individual award of £45,000. It is not unusual for SMART winner to go on to develop a product using a SPUR award.

9.3.3 The Teaching Company Scheme (TCS)

This scheme is more squarely aimed at technology transfer, rather than simply sponsorship of innovation. Recent graduates are made available to companies at a subsidised rate to work on specifically approved projects on two year temporary contracts. The graduates are

partially supervised by HEI teaching staff, while working on a project which is considered to be of benefit to the organisation. The cost of these graduates ranges from £9000 per annum for small firms to £15,000 per annum for those employing more than 250 people.

At the time of writing, it is evident that all of the UK schemes are to be reviewed by the new government, and that this may lead to significant delays in the award of grant-aid to businesses with outstanding applications.

9.4 Schemes in other parts of the world.

The schemes discussed above relate mainly to UK organisations. This section aims to compare those UK schemes to ones used in other countries to encourage technology transfer, and particularly increased adoption of microelectronics.

9.4.1 Methods of investigation

In order to investigate the assistance available to companies in other countries a questionnaire was sent to the Trade Desks of 21 embassies located in the UK. The questionnaire used is reproduced as Appendix D. Following reminders, the response was still not great (8 embassies replied), so further investigation was made using the various government pages published on the World Wide Web.

9.4.2 The 'tiger' economies of South East Asia

The economies of South East Asia are often considered to be the most progressive in support of microelectronic enterprises, and the discussion of world ASIC markets in *Chapter 5* showed that the use of the technology in ASIA and the Pacific Rim is indeed advanced.

Growth in gross domestic product (GDP) of some countries in the area are shown in *Table 9-6* (OTS, 1997), and much of this growth is due to electronic and microelectronic manufacturing industries.

Country	GDP growth in 1996
Laos	7%
Thailand	8.7%
Cambodia	5.5%
Singapore	7.9%
Malaysia	9%
Vietnam	9.5%
Indonesia	7.3%

Table 9-6. GDP growth in South East Asian countries

Examples of support for the microelectronics industry are discussed here in relation to two neighboring and fast growing economies, Malaysia and Singapore.

Malaysia.

Over the last few years, Malaysia has maintained a growth in GDP of over 8%, with around 30% of the GDP being produced by manufacturing industry. (DTI, 1996:2)

However, the country faces significant problems in its high-technology sector. Due to a shortage of labour, Malaysia, although low-cost by western standards, cannot compete using labour rates when compared with some of the more populous Asian countries such as China and India (Bacani and Hamilton, 1997), so instead opted for the introduction of high levels of automation in its factories. However, the country has a shortage of skilled labour and little capacity for research and development. It relies heavily on the manufacture of products designed overseas.

In order to try to overcome this deficiency, the Malaysian government has introduced a number of schemes aimed at increasing technology transfer into its manufacturing base and increasing the extent of local research and development.

The Pioneering Enterprise Scheme for example provides extensive tax-relief for new companies, particularly those engaged in the transfer of technology. The country also allows significant tax-relief (up to 200%) on research and development spending, and exemption from taxation for a period of five years for companies set-up for the purposes of research and development.

Double deduction (200% tax relief) is also available for the costs of staff training in technology related areas, particularly for companies employing 50 or fewer employees. Small companies also enjoy significant reinvestment allowances and total exemption from the payment of customs duties on raw materials, components and machinery which cannot be sourced locally.

The Malaysian Multimedia Supercorridor (MSC) scheme has been established. This scheme uses a number of 'flagship projects' such as the introduction of smart-cards and the building of a 'Cyber-City' in order to encourage the adoption of technology and the growth of development skills. Companies taking part in this scheme enjoy significant tax incentives and government grants.

Singapore.

In 1991, the Singapore government embarked on a five year National Technology Plan with the following aims:

- To promote the increase of R&D expenditure to 2% of GDP
- To have at least 50% of the R&D budget sponsored by industry
- To have a ratio of research scientists and engineers of 40 per 10,000 of the total workforce

This activity was supported by a government R&D fund of two billion Singapore Dollars (\$US1.4 billion).

Singapore supports a wide range of schemes to catalyse technology transfer and the introduction of new technology. Many of these schemes are coordinated by the National Science and Technology Board (NSTB, 1997:1).

Some of the schemes are outlined below:-

- **Broadband R&D Grant Scheme.** This grant scheme is aimed at companies involved in the 'Singapore One' project to introduce broadband communications services throughout Singapore (NCB, 1997).
- **Patent Application Fund.** This scheme exists to help meet the costs of securing intellectual property protection through international patents.
- **Innovation Development Scheme (IDS).** This scheme provides grant aid of up to 50 % of project costs. Eligible costs include manpower related costs, Materials/equipment costs, professional services and Intellectual Property protection costs.
- **Research and Development Assistance Scheme (RDAS).** This scheme provides grant aid of up to 50 % of project costs for projects with significant technological merit. Eligible costs include manpower related costs, equipment costs, training costs, consultancy costs.

- Semiconductor Manpower Development Initiative. This \$30M initiative aims to increase the level of indigenous knowledge of semiconductor related skills. The initiative sponsors a number of routes from post-graduate training to research exchange programmes.
- Research Incentive Scheme for Companies (RISC). This is an investment scheme aimed at helping companies to develop their R&D skills in strategic technologies.
- IT Cluster Development Fund
- Double Deduction for Expenditure on R&D For Services Project
- Investment Allowance Scheme
- Pioneer Status Incentive. Tax incentives for new companies

The government also sponsors four research institutes specialising in microelectronics, systems science, information technology, and wireless communications. These institutes are involved in joint R&D projects with industrial partners (NSTB, 1997:2).

As a result of the National Technology Plan, in five years, the country has achieved most of its initial targets (Kian, 1996). R&D spending only reached 1.1% of GDP, but this was against a high growth rate (up to 15% per annum). The ratio of scientists and engineers reached 45 per 10,000 of the workforce, and the private sector contributed 65% of R&D funding. Clearly, a well structured and adequately funded industrial policy can have remarkable success in increasing the technological base of a country's industry.

In terms of the Spence model discussed in *Chapter 8* Singapore has produced a technology transfer infrastructure capable of supporting the needs of new adopters at every stage of the

adoption process from early information to significant financial aid at the point of implementation.

9.4.3 Hong Kong

One initiative identified in Hong Kong was the Applied Research and Development Scheme. This scheme, sponsored by the Hong Kong government, provides loans of up to 75% of the development and marketing costs of innovative products. Loans are repayable later in the product lifecycle. This is more of an example of a government initiative to bring venture capital in contact with innovative companies than a scheme particularly involved in technology transfer, but the loans have been used by companies in order to introduce ASIC technology. It is presently unclear whether this initiative will survive the political changes due in Hong Kong in 1997.

9.4.4 Israel

The support of industrial research and technology transfer in Israel is set in law. The law For Encouragement Of Industrial Research And Development came onto the statute books in 1984 and had three main objectives (MIT/OCS, 1996):-

- To foster the development of local technology-orientated industry through utilising and expanding the country's existing technological infrastructure
- To improve Israel's balance of trade by increasing manufacture and export of high-technology products
- To create employment opportunities in industry and exploit Israel's highly capable scientific and technological labour force

In support of these objectives, a Research Committee made up of representatives of government, industry and academia are able to award development grants of between 30% and 60% of the R&D costs of a new product. Products that are successful must later repay the grant through royalties on product sales. These royalties are then used to fund future grants awarded under the same scheme.

Israel also operates a number of international research agreements and contributes to and takes part in the EU's collaborative research programme (Framework IV)

More specific to microelectronics development is the Magnet Programme. This programme aims specifically to disseminate new technologies (including microelectronics) in addition to providing grants to aid in pre-competitive research. Since its introduction in 1992, Magnet has sponsored 14 collaborative research and dissemination projects.

In order to stimulate start-up industries, particularly among recent immigrants, the government sponsors a number of 'Technological Incubators'. The companies based at these incubator centres (which might to some extent be considered similar to science parks) are able to apply for grants of up to 85% of approved budgets up to a maximum of \$US500,000 over a two year period. To date approximately 200 projects are being supported at 27 technology incubator centres (MIT/OCS, 1995).

So it can be seen that in relation to the models discussed in *Chapter 8*, Israel is attempting to encourage some new-user companies through all stages of adoption, although this support is generally provided as part of its repatriation programme. Through its establishment of technology incubators, it also aims to develop the type of formal and

informal linkages inherent in the Rothwell & Zegveld model (see *Figure 8-7*). Interestingly, and perhaps unique, is the approach to making the grant support system self-funding through the payment of royalties on successful products.

9.4.5 Other replies to the embassy survey.

In addition to the detailed information provided either through direct responses or review of web pages, the following responses were also received from the embassies surveyed.

Country	Response
Morocco	No specific support for microelectronic technology
New Zealand	Although no specific schemes in support of microelectronics, the country does run a 'Technology for Business Growth' scheme that pays up to 50% of R&D cost of suitable projects.

Table 9-7. Other embassy responses

9.5 Conclusions on technology transfer schemes

It is evident from the wide variety of technology transfer schemes discussed in this chapter that different countries place significantly different emphasis on the importance of technology transfer in their industrial strategy. The UK does not appear to have a consistent 'industrial policy' preferring to leave industrial development largely to market forces. In areas where specific market failures can be identified, small, specific intervention schemes such as Microelectronics in Business are put in place, and given their relatively small budgets are very successful and certainly good value for money.

The EU also follows a policy of minimum intervention. The Europractice initiative is a good example of limited intervention, but it can only be considered to be an incomplete approach due to it only supporting a few companies at a very limited point in the adoption process.

Other countries, including the so called Tiger Economies, have wide-ranging industrial development policies which are in some cases (e.g. Malaysia and Israel) enshrined in law. These strategies are often supported with high levels of financial support, and have been shown to be particularly successful in reaching their stated aims. Although not limited to the adoption of microelectronics, these support schemes have been shown to have encouraged significant increases in the microelectronics content of their countries products.

10. Comparison with another industry.

The major part of this study has addressed technology transfer with particular emphasis on ASIC adoption. It is useful to consider whether the case of ASIC technology is a unique one or whether there are similar characteristics in the adoption of other new technologies in other industrial segments.

The industry chosen to perform comparisons with is the Biotechnology Industry. In common with ASIC technology, the success of biotechnology requires that a new technology be adopted across a wide range of traditional industries in order to enhance the products of that industry. In addition, biotechnology contains examples of competence-destroying discontinuities in technology which have caused a step-change in the technology and methods available to companies operating within a range of industries in much the same manner as the introduction of commercially available microelectronics has influenced industries that have the ability to use electronics in their products.

10.1 Biotechnology

The so-called 'new' biotechnology is a technology that has emerged in the post-war period based on the introduction into biology of a number of other scientific disciplines (e.g. physics, mathematics). This has enabled the description of life processes at the cellular and molecular level (Smith, 1996). The technology has found application across a wide range of industries as diverse as brewing and pharmaceuticals. This is summarised in *Figure 10-1*. Unlike single scientific disciplines, biotechnology can draw upon a wide range of supporting sciences such as microbiology, immunology, and cell biology and supporting engineering processes such as electronics. The technology might best be described as the application of biological organisms, systems or processes to manufacturing and service industries.

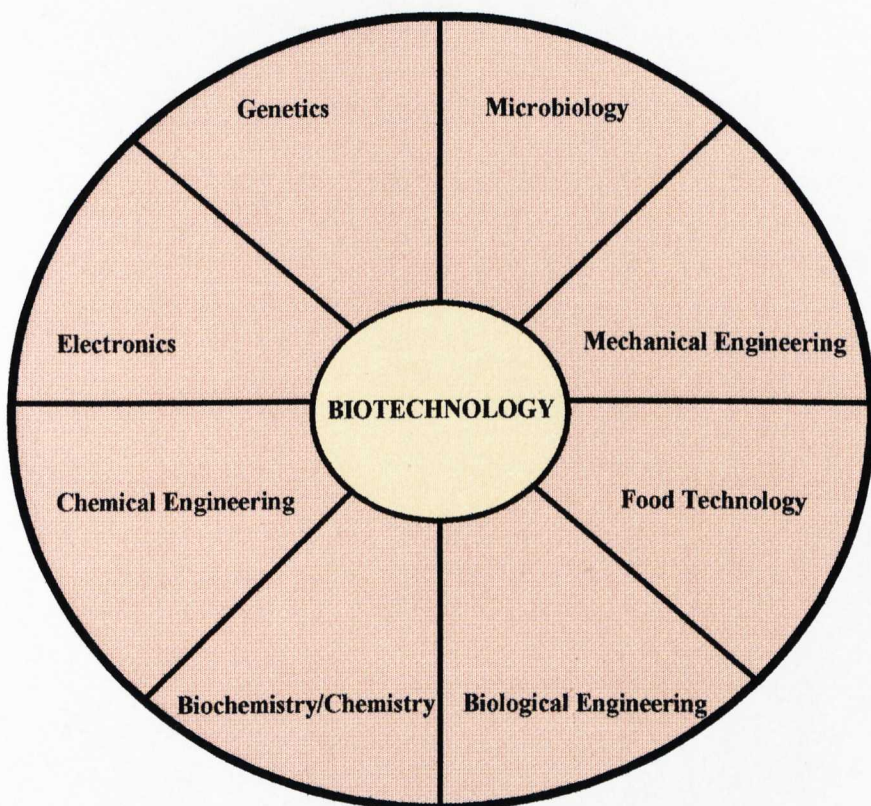


Figure 10-1. The interdisciplinary nature of biotechnology

The history of biotechnology is a long one, originating in the biological production of food and beverages. There is evidence of beer having been brewed as early as 6000BC. The technology has evolved through the development of biological processes in non-sterile conditions (e.g. the production of ethanol by open fermentation in the late nineteenth century) and the introduction of sterility to biotechnological processes (e.g. the production of antibiotics and monoclonal antibodies (MAbs) since the 1940s) to today's state of applied genetics and recombinant deoxyribonucleic acid (r-DNA) technologies, which allow the biological properties of organisms to be 'programmed' (Smith, 1996). In comparing biotechnology with ASIC technology we will concentrate on the adoption of the so called 'new' biotechnologies (e.g. r-DNA and MAbs). These developments have allowed products such as synthetic insulin and Interferon to be commercially produced (Check, 1994)

10.2 Industry Structure

A number of studies have shown that a networked industry has emerged comprising of universities, research hospitals, large firms and start-up firms established specifically to exploit biotechnology (the dedicated biotechnology firm (DBF)) (Dodgson, 1993). The biotechnology industry is dominated by large companies. Although a number of entrepreneurial start-up companies have emerged, they have not been able to replace the large traditional companies in the way that fabless chip companies have in the microelectronics industry. This is due largely to the existence of some particularly high entry-barriers to the exploitation of a new product that exist for biotechnological products. For example, in the pharmaceutical market, it is estimated that the development and introduction of a new drug may cost in excess of \$200 million due to some extent to the regulatory framework that exists for new drugs (OTA, 1991). Clearly, a start-up company would find such a sum difficult to raise. Large companies however, while having significant funds, do not have the adaptiveness and flexibility inherent in the smaller DBFs, or innovative internal research of the type undertaken in universities. (Arora & Gambardella, 1990). Take-overs, mergers and failures do of course take place, but the structure is far more one of a symbiotic network. This is illustrated in *Figure 10-2*.

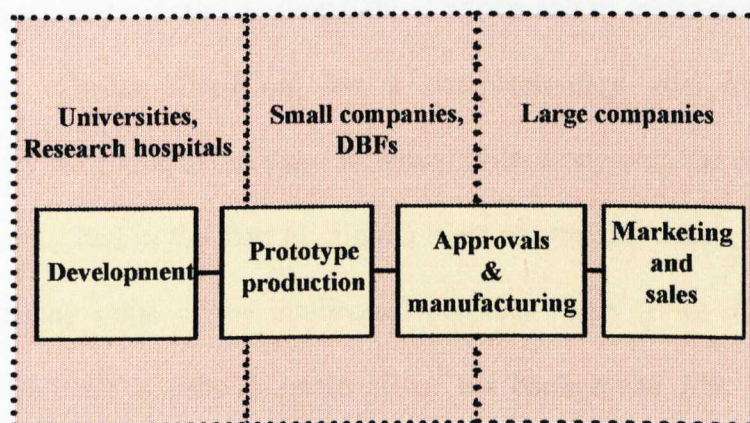


Figure 10-2 Collaboration in Biotechnology

It can be noted that this structure fits well with that proposed by Rothwell and Zegfeld (see *Chapter 8*). They propose that the nature of innovation is that of the exploitation of a network of differing skills and social needs in the production of a product to suit a particular market need. This was discussed more fully in *Chapter 8*, and exemplified in the case study described here.

10.2.1 Case Study - Celltech/American Cyanamid.

In his discussion of collaboration and innovation, Dodgson (Dodgson, 1993) relates the case of Celltech and their collaboration with American Cyanamid.

Celltech are a DBF based in the UK who after entering into a research contract with American Cyanamid in 1986, progressed to create a cooperation agreement in 1990. Celltech had been formed in 1979, and although by 1991 its turnover had grown to £17million, its research budget was over £10million. This high proportion is indicative of the technology which requires a high degree of investment. As a result, Celltech had only made an operating profit in one year of its history.

Celltech is a world leader in the development of MAbs and in particular in using them to combat specific cancers. Cyanamid has a complementary skill in toxins, and in collaboration they were able to use these technical skills along with the marketing skills of Cyanamid. This resulted in the start of clinical trials of two anti-cancer drugs in 1992. In addition to retaining some of the intellectual property rights (IPR) in specific product developments, Celltech is able to retain all of the background IPR developed in the projects (in this case all IPR relating to non-cancer applications) and so give themselves a base for future product developments.

10.2.2 Strategic approaches of emerging biotechnology firms.

In pursuing their wish for growth and commercial success, emerging biotechnology firms have followed a number of strategies (Hamilton, Vilà and Dibner, 1990). Those strategies evolve over time and have been analysed in relation to:

- Innovation focus - The importance of upstream (research and development) and downstream (manufacturing and marketing) innovation activities in the firm's strategy
- External orientation - The extent to which strategic alliances and other external arrangements are considered key to the firm's strategy
- Timing - The way in which the balance of the two aspects discussed above changes with time.

The study performed by Hamilton, Vilà and Dibner reviewed the strategies of new biotechnology companies over time. They reviewed the balance of innovation focus and external orientation at the time of formation, the time of the study (an average of seven years after formation) and that predicted for five years after the study. The results are summarised in *Figure 10-3*.

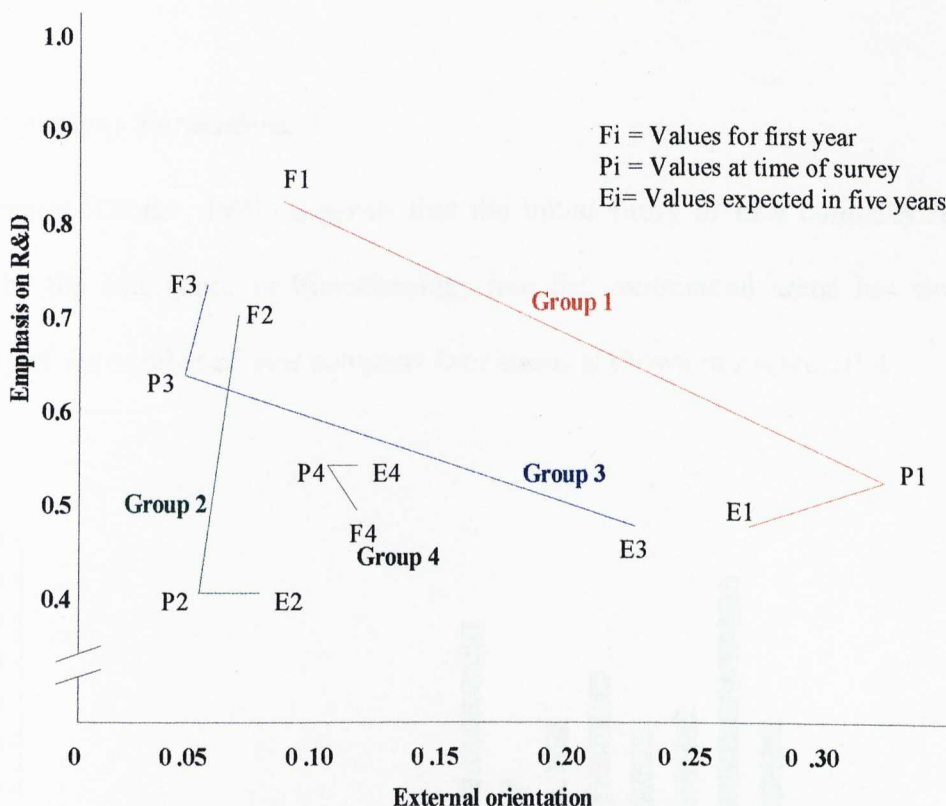


Figure 10-3. Emerging strategies of firms

The implication of the results of this study is that while a number of different strategies exist, in most cases companies reduced their dependence on R&D as the firm became more established, and instead concentrated on building downstream activities such as manufacturing and marketing. This change may be performed either by the growth of internal resources (as in group two of *Figure 10-3*) or by increasing reliance on external collaborators (group one). The time at which companies make this transformation varied from group to group, with some companies (group 3) handling much of their internal development internally, but realising that an increase in external activity would be required in their future. The fourth group of companies made and planned little change in strategic focus, and were generally considered to be small, market-driven, niche-market companies concentrating on single products. At the time of the survey, it was not evident whether any one strategy was inherently more successful than another.

10.2.3 Company Formations.

Mark Dibner (Dibner, 1991) suggests that the initial flurry of new company formations caused by the emergence of biotechnology into the commercial arena has slowed. His summary of the number of new company formations is shown in *Figure 10-4*.

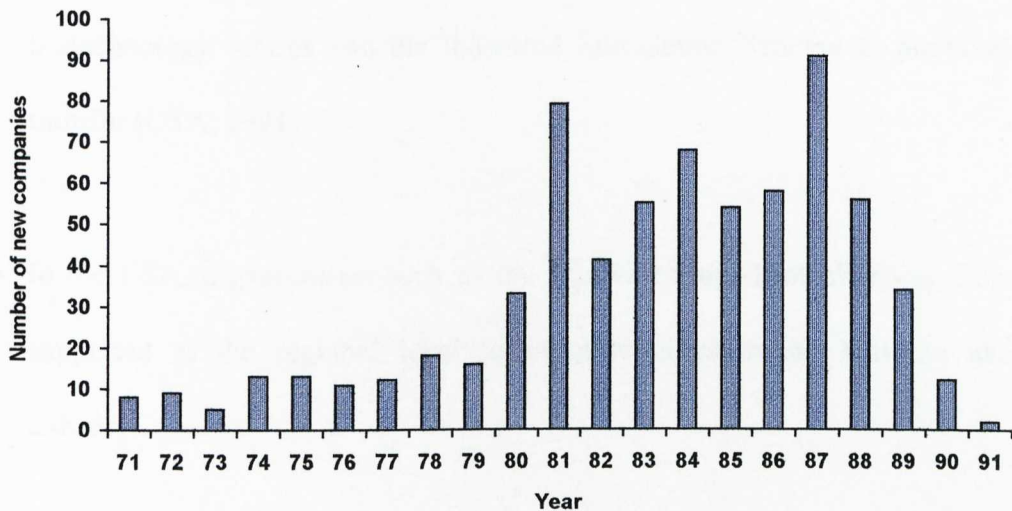


Figure 10-4. Formation of Biotechnology companies in the USA

This distribution fits well with the suggestion that an initial flurry of company activity following the introduction of a ‘disrupting’ technology (i.e. one that challenges the core competences of traditional industries) eventually tails off to be replaced by amalgamations, joint ventures, mergers and company closures as the market stabilises. In the case of biotechnology, this seems to have taken place over a relatively short period.

10.2.4 Government intervention in biotechnology

As with ASIC technology, the role of government has been important in increasing adoption. Realising that the inter-disciplinary nature of the technology would cause

difficulty in its adoption, a number of governments have initiated technology transfer schemes (Dodgson, 1993).

- In Japan, the Ministry of International Trade and Industry (MITI) sponsors the Japan BioIndustry Association and the Research Association for Biotechnology.
- In the Netherlands, the government sponsors a number of university based biotechnology centres and the Industrial Stimulation Scheme to promote technology transfer (OTA, 1991)
- In the USA, organisations such as the Midwest Plant Biotechnology Consortium are supported at the regional level to promote collaboration between academia and industry.

In the UK, responsibility for government involvement in biotechnology lies with two main bodies. These are the Biotechnology Unit of the DTI, and the Biotechnology and Biological Sciences Research Council (formerly the Biotechnology Directorate of the Science and Engineering Research Council (SERC)).

The Biotechnology unit was formed in 1982 and has encouraged a number of initiatives under the DTI's LINK programme. No specific awareness raising activity comparable with Microelectronics in Business has taken place, but a number of specific development projects have been funded (e.g. the Eukaryotic Gene Manipulation Programme). This is perhaps analogous to the FUSE programme of the EU in microelectronics. A number of

‘clubs’ such as the Biosep Club, which concentrates on those interested in bioseparation techniques, have been formed and supported.

The Biotechnology Directorate of SERC was formed in 1981, and has more recently merged with part of the Agricultural and Food Research Council (AFRC) to form the Biotechnology and Biological Sciences Research Council (BBSRC). The BBSRC concentrates on the promotion of long-term research so as to generate a pool of technology on which industry can draw. The council also promotes a number of ‘clubs’ in areas such as Protein Engineering, Antibiotics and recombinant DNA. (Cabinet Office, 1994). Although primarily aimed at the academic sector, the BBSRC does claim to be active in a number of industrial projects, and claims to interact with over 200 companies including Zeneca, Pharmaceutical Proteins Ltd, Rhône Mérieux and Piman-Moore.

10.3 Adoption of Biotechnology.

The adoption of biotechnology has much in common with that of ASIC technology for a number of reasons including:

- The technology is applicable across a wide and disparate range of industries and products. However, this range is not as wide as that of microelectronics, and is consequently easier to identify and apply marketing efforts to.
- Knowledge of the technology would not be resident in many organisations that might use it.
- A number of 'myths' about the high cost and risk of adopting the technology have emerged. In the case of biotechnology this includes a high level of public concern over genetic manipulation. Rumors concerning high costs of adoption appear to be founded in fact.

There are however also some significant differences between biotechnology and ASIC technology:

- Most advances in biotechnology have been made in university research establishments rather than in industry, so the extent of technology transfer needs to be higher than in microelectronics.
- The level of initial investment required to exploit biotechnology is often significantly higher than that encountered in microelectronics and lower entry-level technologies are rarely available at costs suitable for the adoption by SMEs alone.

10.4 Conclusions on biotechnology.

The biotechnology industry may in some respects be considered to be younger than microelectronics, but has progressed at a different rate through some stages of its evolution. In some respects, some of the early traits of the microelectronics industry are evident in biotechnology.

Entry costs are still very high, and pay-back periods long, so the availability of the technology to SMEs is limited to those with large capital budgets or access to support from or collaboration with major companies. However, there are many rumors of an imminent 'boom' so SMEs (DBFs) are being formed to exploit the work being performed in universities. Venture capitalists are becoming interested in an attempt to mimic the large profits that were made in the early years of the microelectronics industry.

At this stage, the technology does not exist in a form that is suitable for wide-scale adoption, so specific government initiatives aimed at increasing such adoption would be premature. Government initiatives aimed at developing core skills that can later be exploited by industry are more in fitting with the current technological situation.

Having been born in the era of the 'networked company' many new DBFs may remain in that state, choosing to concentrate on their core competences. As the technology matures, it may be that a reduction in the numbers of DBFs takes place as larger companies develop in-house capability if suitable low-cost technologies become available. This is analogous

to the increase in in-house development of digital ASIC devices that has coincided with the availability of FPGA technologies.

Comparisons can be drawn between the emergence of small entrepreneurial companies in the two industries. In biotechnology, these start-up companies have quite quickly been absorbed by large companies. This has occurred to some extent in microelectronics, but the lower cost of entry has enabled a continual stream of new companies to continue to be established and be successful in microelectronic related industries. As more sectors of industry adopt microelectronics, and new microelectronic products emerge, there will continue to be opportunities for success for small companies in niche markets. If the fall-off in the rate of establishment of biotechnology companies suggested by Dibner (Dibner, 1991) is maintained, it would appear that opportunities for small companies to exploit biotechnology are diminishing.

11. Conclusions and implications.

There are a number of overall conclusions that can be drawn from the various aspects of this study regarding the status of ASIC adoption in the UK. These conclusions relate particularly to the SME manufacturing base although many of them also have significance to larger companies. If these conclusions are accepted, there then appears to be a number of routes that might be taken by industry, government and other stake-holders in order to increase adoption of ASIC technology. The conclusions also have number of implications for the generally accepted models of technology adoption.

11.1 Conclusions.

The use of the term ASIC to describe a type of technology is in itself controversial. Different elements of the design and supply industry apply the definition differently in order to enhance the standing of their own products or to denigrate the qualities of others. This vagueness of definition has not been helpful to the industry at large as it has increased the level of confusion in potential users. In essence, the best definition of an Application Specific Integrated Circuit is,

'An integrated circuit which is specifically designed and manufactured to perform the requirements of one specific application or product'

This definition can then cover any type of technology which results in the production of a chip for a particular product, irrespective of whether the customisation of the chip to the application takes place at a silicon foundry or on the user's production line. This definition is necessary due to the large and constantly changing range of ASIC base-technologies (e.g. gate-array, FPGA) and the overlap between such technologies which make any other definition difficult to apply.

New ASIC base-technologies (e.g. programmable analogue devices) have emerged during the period of this study, and will inevitably continue to emerge in the future. However, some constant rules do apply. All of the technologies studied, when taken in isolation, tend to show classic experience curve, and product life-cycle effects. This allows the prediction of likely future cost and sales volumes for emerging products.

The emergence of ever newer, faster, cheaper base-technologies also means that there is an increasing probability that a good match can be found between a potential users application and an available technology. Key to the emergence of suitable new technology has been the growth in the number of programmable technologies available to meet low-volume requirements and reduce 'time to market' at a time when the life-cycle of products is getting ever shorter. It is always worth remembering that the product life-time of some products is now shorter than their development time (e.g. mobile phones or PC motherboards). This will bring increasing pressure on designers to adopt methodologies which can reduce development timescales.

Some interesting conclusions can also be drawn regarding the nature of manufacturing industry in the UK in the mid-to-late 1990s. The 1970s and 80s saw a dramatic change in the UK manufacturing base. During the 80s the UK industrial base suffered a severe recession. Almost all manufacturing industry sectors experienced significant pressure to cut costs and become more globally competitive. Many companies could not adapt and so ceased to exist. Many large companies shed significant levels of staff in so called 'downsizing' initiatives. While one might argue with the prudence of these initiatives, and of the UK government in allowing and encouraging such action, it has had a number of significant results.

Firstly, the UK has moved further towards a manufacturing base made up largely of SMEs. The proportion of SME companies in some industry sectors (e.g. electronics) is higher than in many competitor nations. Many of these SMEs were formed during the industrial recession or fought hard to survive it. As a result, much of the dead-wood traditionally associated with UK industry has disappeared, leaving an SME base which is more flexible,

innovative and ready to adopt change. This was supported by the views of the ASIC design industry, who see their SME clients as more flexible and adaptive than their large industrial clients. However, such companies are also seen as being severely undercapitalised, and so often unable to invest in the new technologies which might enable them to compete in global markets.

The structure of UK companies is also changing. Due to the need to adapt quickly to changing market needs, while minimising the cost of such changes, many companies are adopting a 'networked company' structure and forming close relationships with supplier companies rather than trying to maintain in-house expertise in all of the areas necessary for their operation.

This transition to an SME based industrial economy, and the moves toward networked organisations are not unique to the UK. Such transitions are occurring world-wide, and governments are starting to recognise the importance of the SME sector in all areas of industry. This is resulting in increased interest in supporting the growth of SMEs which is reflected in the emphasis of government industrial support initiatives (Cabinet Office, 1996).

In spite of the pressures of recession and changing markets, many small companies have been successful in using ASIC technology to bring them sustainable competitive advantage. A number of such companies are discussed as case studies in *Chapter 3*. A number of similarities exist between these companies, including their readiness to use external assistance in bringing innovative products to market. All of them are, or are becoming, networked organisations in the way that they do business. With regard to ASIC technology,

the successes shown by the companies in the case studies are not confined to one particular type of ASIC, but show examples of all of the base-technologies discussed in this study.

Using systems-based techniques to analyse the ASIC market and its customers leads to the conclusion that a complex and constantly changing environment exists. The suppliers, users, and support agencies (e.g. government) are constantly shifting as changes in technology change the importance of different players. For example, as tools for designing digital technologies become more advanced, the need to use external experts to design them diminishes in favour of internal design teams, and as the programmable devices become more of a commodity, the use of distribution companies to sell them becomes more realistic. This ever-changing system makes the analysis of adoption a difficult one, and one which is unlikely to have clear-cut conclusions.

Some conclusions regarding the nature of the market may however be made. It is undoubtedly true that the World, European and UK markets for all types of ASIC device are growing at a remarkable rate. Occasional glitches in growth do occur as fluctuations in supply and demand lead to the now recognised 'silicon cycle', but any fall off in demand has traditionally led to a price led response from the semiconductor industry which has often led to the next boom in a particular product area (e.g. PCs and perhaps digital TV in the near future).

However, the study shows that the UK has not been keeping pace with the advances in microelectronic technology when compared either to its European or World competitors. In *Chapter 5* it was shown that the UK SME base might account for perhaps 20 masked ASIC design starts each year of 200 performed in the UK and 2000 performed in Europe at

large. However, even Europe falls behind world trends when these figures are compared with the 7000 design starts per year seen in the emerging economies of the Pacific Rim. This usage rate in the Pacific Rim should be viewed alongside GDP growth rates of around 6-8% fueled largely by manufacturing industry, and a perceived importance of the growth of SMEs within many of these countries.

Increasing the adoption of ASIC technology within the UK SME sector provides a difficult problem for the UK supply industry. It should also be noted that much of the supply industry is itself embryonic and faces a constantly shifting and dynamic market. The role of semiconductor manufacturers, design houses and distributors is constantly changing as new technologies emerge, but one constant pressure comes from the need to apply marketing budgets in areas in which they are most likely to succeed.

Unfortunately, these areas do not include the SME sector. The disparate nature of the market, the spread of industries, and the vast range of potential applications when coupled with a lack of investment capital means that suppliers will inevitably move their attention away from the SME base towards more lucrative contracts with large companies where the chances of repeat business are also higher. Opportunities to do business in the SME sector certainly do exist, but the business development plans of most UK suppliers (particularly design houses) tend to favour addressing large customers in export markets rather than addressing the UK SME base.

Before adoption of ASIC technology can be encouraged in the SME base, there are a number of obstacles to be overcome. The surveys performed for this study, and the review

of earlier studies show that perceptions about ASICs held by the SME base have not altered significantly in recent years. In essence, large numbers of potential users still believe that ASICs have the following characteristics:-

- High cost of entry and use
- High risk of failure
- Problems of single-sourcing
- Problems of insufficiently trained staff
- A requirement for high production-volumes

When each of these perceptions is taken in isolation, it can be shown that they are either wrong or at least of no greater importance than concerns that exist in many areas of a company's day to day operation. *Chapter 7* discusses these areas in detail, but the conclusion is that there is not any single all-important reason preventing an SME from adopting ASIC technology. The reasons must then be a wide range of small problems and perceptions which when added together prevent adoption. However, the power of perception should not be underestimated, and neither should the effort involved in changing such perceptions.

In order to evaluate the situation in some detail, *Chapter 8* reviews a number of models. Earlier analysis had suggested that a 'soft' or 'messy' situation exists so systems models are used to clarify the situation. Important in the conclusions to be drawn from these models are:-

- The situation is a complex one with no single answer

- Different phases of adoption require different support structures
- Organisations exist as political systems and organisms
- Communication between parties is key to adoption
- Methods of easing the step-change associated with ASIC adoption might increase uptake

Clearly, a 'market failure' exists. Consequently, if UK government believes that manufacturing industry is important to the future prosperity of the country, then there is a role for it to play in supporting increased adoption of new technologies by the manufacturing base. Two major questions are:

- To what extent should intervention be taken?
- To what extent should market forces be allowed to prevail?

Chapter 9 reviews a number of UK, European and overseas government initiatives in the light of these questions.

There is a wide spectrum of government intervention strategies at work in the world-wide ASIC market ranging from the minimalist intervention seen in the UK and Europe with initiatives such as Microelectronics in Business and Europractice, through to the full-blown industrial strategies enshrined in law that are evident in South East Asia. The level of financial subsidy also ranges from the thinly-spread, wide-area approach of MiB, through the limited-participant capital support of schemes such as FUSE, to wide reaching support such as the \$2 billion available to companies in Singapore (a country the size of the Isle of Wight) through just one of its intervention schemes.

To a large extent, the scope of these schemes is defined by the availability of resources in the various countries (Singapore has a \$15 billion trade surplus), but in addition, developing countries with clear national industrial development plans such as Malaysia are being successful in stimulating industry, and this has resulted not only in significant growth rates in GDP from a low initial base, but in high GDPs in absolute terms. Much of this growth is based in industry, and a high proportion of that is in the electronic manufacturing sector.

While schemes such as Microelectronics in Business and Europractice may be considered to be very successful when considered in relation to the limited budgets that they have available, they cannot be considered to form any part of a consistent industrial policy with clear objectives, reflecting instead the laissez-faire attitude to industry and the emphasis on a market-led economy evident in most UK government policy since the 1980s. The result of this is the inevitable loss of world market share to the more dynamic members of the 'Tiger Economies' of South East Asia. To some extent this inevitability has been accepted by UK government in its recently launched 'South East Asia Campaign' which aims to increase UK exports to what it sees as the worlds fastest growing economies. The campaign also promotes ways in which UK companies can become involved in overseas government sponsored technology transfer initiatives such as the Malaysian Multimedia Supercorridor and its supporting technology development programmes (Arif Nun, 1997).

The situation in microelectronics could be considered to be unique, so in order to investigate its uniqueness, a short study was made of a technology which is often considered analogous to microelectronics. Biotechnology is often cited as the 'the next

technological revolution' and appears on the face of it to be similar to microelectronics in that its applicability spans a wide range of industry, and that it requires a high degree of technical ability to implement. However, the structure of the biotechnology industry has been significantly affected by the environment in which it operates. The high level of government intervention and regulation involved for example in the approval of a new drug has imposed massive entry barriers to biotechnology products, so while small companies have emerged to develop technology, they are inevitably swallowed up or amalgamated with larger entities as products get nearer to the market. Low-cost methods of exploiting biotechnology are yet to be developed.

There are few technologies that can claim to have the far reaching effects of microelectronics. Microelectronics are now used in many products that we use daily, from motor-vehicles to alarm clocks; from PCs to toasters. This study has shown that this all-pervasive nature of the technology can only increase in the future. While some of UK industry has embraced the technology and used it to its advantage, much of the industrial base has not, and is falling behind its overseas competitors. While government has recognised this failure for some years, it has done little to encourage higher levels of adoption due to limitations of resource and lack of political will to intervene in the market.

The supply industry is successful in its own right, but gains much of that success in working with overseas users and large manufacturers rather than the UK SME base. This is a matter of business expedience and is unlikely to change. Change, if it is to come about, must either be organic, originating in perceived need from individual companies, or should be encouraged by government, trade associations, and other non-profit organisations. Time however is running out. While UK industry vacillates, the emerging economies of other

areas of the world are seizing the opportunities presented by microelectronics and creating successful economies predicated on technology adoption.

11.2 Implications for stake-holders in the ASIC market

The conclusions above may seem somewhat disheartening from the view of UK industry, but a number of routes to increasing adoption of ASIC technology are evident which could significantly improve the prospects of adoption in companies within the UK who could benefit from the use of the technology. These routes to increased adoption involve activity from a number of the stake-holders that have been identified in the course of this study.

While it is unlikely that any single initiative by a single group could be assumed to bring the market to a position where a 'critical mass' of adoption would result in a self sustaining system, a combination of activities by a number of groups might be sufficient to bring the group of potential users to such a state. Initiatives that might be taken by individual groups are discussed below.

11.2.1 Implications for industry

In reviewing these implications it should be remembered that the UK ASIC design and supply industry is a successful industrial sector in its own right. UK design companies perform a significant proportion of their work for overseas companies and so represent a source of export revenue. Some are also forming joint-venture partnerships with overseas manufacturing organisations which will also indirectly bring revenue to the UK.

However, many UK design and supply companies see the UK SME base as a fruitless market which is unlikely to lead to significant business. This has been shown not to be the case by some companies who have been able to target specific segments of the market and

who have been able to amortise the high cost of sale over longer term repeat business or in the provision of further added-value services. Examples of this are the design companies who are offering 'design and supply' services for new users of electronics.

The UK design and supply sector would do well to reconsider their marketing approaches to the SME base in the light of this and consider ways of flexibly tapping into what remains a large and untapped market. Useful marketing approaches might include commitment to and participation in government initiatives, user-groups and professional-institution based promotion schemes, and the review of alternative first-stage marketing initiatives such as the use of the Internet.

11.2.2 Implications for government

The degree to which government is prepared to intervene in a market is clearly key to the extent to which they will be prepared to try to encourage the adoption of microelectronics in the UK SME base. At the time of writing, shortly after a General Election, it is unclear to what extent the political will to intervene might change in the future. However, the work of this study has shown that a market failure exists which is unlikely to cure itself in the short term. It may be that, given time, UK industry will realise that it has no alternative but to adopt microelectronics in its products. But time is short. Overseas competitors are already reaping the rewards of increased adoption and will continue to build a market presence that may become unimpeachable. This market failure can be addressed through government intervention, and by an increase in support to SMEs wishing to adopt ASIC technologies.

In the recent past, UK government has had little clear policy with respect to manufacturing industry. At one point it appeared that such industry had been abandoned in favour of a service-industry economy. However, recent trends suggest a slight change of heart in favour of support of manufacturing industry. If this industrial sector is to survive and flourish, it must adopt new technology and use it to its advantage. Microelectronics is a key technology for many industrial sectors, so support of its adoption should be key in any industrial policy. This is certainly the case in the successful industrial economies of the Far East, and the UK ignores it at its peril. While budgetary constraints may prevent the high levels of support evident in other nations, failure to provide sufficient support can only result in a lower level of technology adoption and a less successful manufacturing base.

However, even with a limited budget, intervention of the type performed under the MiB programme could continue. The establishment of support centres, business advisors and user-groups that has already taken place under this programme has been key in increasing adoption, and could continue to be key in the future.

11.2.3 Implications for Educational Establishments and Professional Bodies.

The study of the content of engineering degree courses identified a shortfall in these courses in relation to the development of the business and commercial skills necessary to successfully introduce ASIC technology into a company. While graduates will have sufficient technical skills to begin ASIC designs, they are not able to become Technology Champions. This would suggest that an increase in the level of commercial training given in degree courses would be useful. However the normal three or four year first-degree course already has difficulty in including all of the technical subjects necessary, and any increase in business subjects would have to be at the expense of some other content. So,

while an increase in business training at first-degree level is desirable, it may be that the most appropriate place for such training is at the post-graduate level.

Currently, only a small proportion of UK electronic engineers pursue higher degrees, so while increased business training could usefully be included in such degree courses, it is likely that a different approach to post-graduate training would be necessary to meet the needs of the majority of UK engineers. The Continual Professional Development scheme of the IEE provides one such route. The scheme is fairly young, and adoption by the engineering fraternity has not been high. It may be necessary to find ways of making such schemes more attractive to engineers, perhaps by making them lead to a formal post-graduate qualification.

Professional institutions might also play a greater role in the initial promotion of new technologies. The special-interest groups and user-groups which have been shown to be useful in building awareness and supporting initial adoption could fit well within the framework of a professional institution, and would be unlikely to be influenced by commercial bias. Such commercial independence has been seen as key to the success of support centres operating within the MiB scheme discussed in the study.

11.2.4 Implications for SME companies.

While the supply industry and other stake-holders must take some blame for failing to promote ASIC technology to the SME base, they cannot be held solely responsible. Some blame for not adopting new technologies appropriate to future success must be attributed to the manufacturing companies themselves. When compared, for example, to the

companies of the tiger economies of the Far East, UK companies are slow to change and very conservative in their approach to risk. In relation to ASIC technology, companies should be increasing the attention that they pay to emerging technologies, and particularly those being adopted by their competitors. Eventually, an industry will get to the stage where adoption of a new technology is unavoidable, but in delaying adoption until this time, companies will have missed significant opportunities and may even find that their competitors have built an unassailable lead.

In order to avoid this situation, it is necessary for SMEs to find ways of building their internal competences in the use of technologies that will be useful to their products. There are a number of approaches to this which do not need to include bringing advanced design or manufacturing capabilities in-house. This study gives examples of a number of companies that are building external networks which allow adoption of new technologies. The main new competences that these companies need to develop are in the management of external relationships. Having established such skills, the companies can progress to using any number of advanced technologies through changing relationships with 'best in class' suppliers.

11.3 Development of models

The study uses two main types of model in assessing the nature of technology adoption. The first set are marketing based and relate to the needs of companies to produce competitive products. These models can be applied to both the adopting companies and their suppliers. The second set are more concerned with the mechanics of technology adoption and in general consider the needs of the adopting organisation. While both sets contribute to the understanding of the situation, both also have weaknesses which might usefully be addressed. These weaknesses become evident when trying to apply the models to the adoption of a complex technology such as ASICs, and to complex and ever-changing markets such as those encountered in electronic products..

The marketing based models, such as those of Porter discussed in *Chapter 3* can usefully describe how products using ASIC technology might be successful, but to some extent fail to address the complexity of real markets and real products. It is often difficult to define a single, analyzable market for a product, and also virtually impossible to define the features that might be possible in a new product without an understanding of new technologies that might be used to achieve them. The marketing models lead one towards a 'marketing pull' rather than 'technology push' approach to new product definition, when in reality some degree of both is necessary.

Some weaknesses also became evident when attempting to apply the adoption models to a real-life market. One comprehensive model of the technology adoption process is that of Spence described in *Chapter 8 (Figure 8-6)*. While this model clearly describes the process of adoption, it assumes that support for the various stages will be readily available if a market for the technology exists. In the case of ASICs, such a hypothesis falls down

because although a large potential market does clearly exist, exploitation of the market is unlikely to take place until it becomes economically viable for suppliers. This requires a 'critical mass' of adoption to be reached so that suppliers no longer need to be involved in activity which is best described as 'missionary'. Until this point is reached, the adoption process must be supported by organisations which do not need to profit from the market in order to survive. These may either be non-profit making organisations such as trade-associations or government departments, or, perhaps less likely, could be organisations taking a much longer-term view of potential returns. If such organisations do not intervene, the adoption process may fail, in spite of the existence of a large potential market.

An amalgamation of market and adoption models applied to a complete group of adopters is shown in *Figure 11-1*.

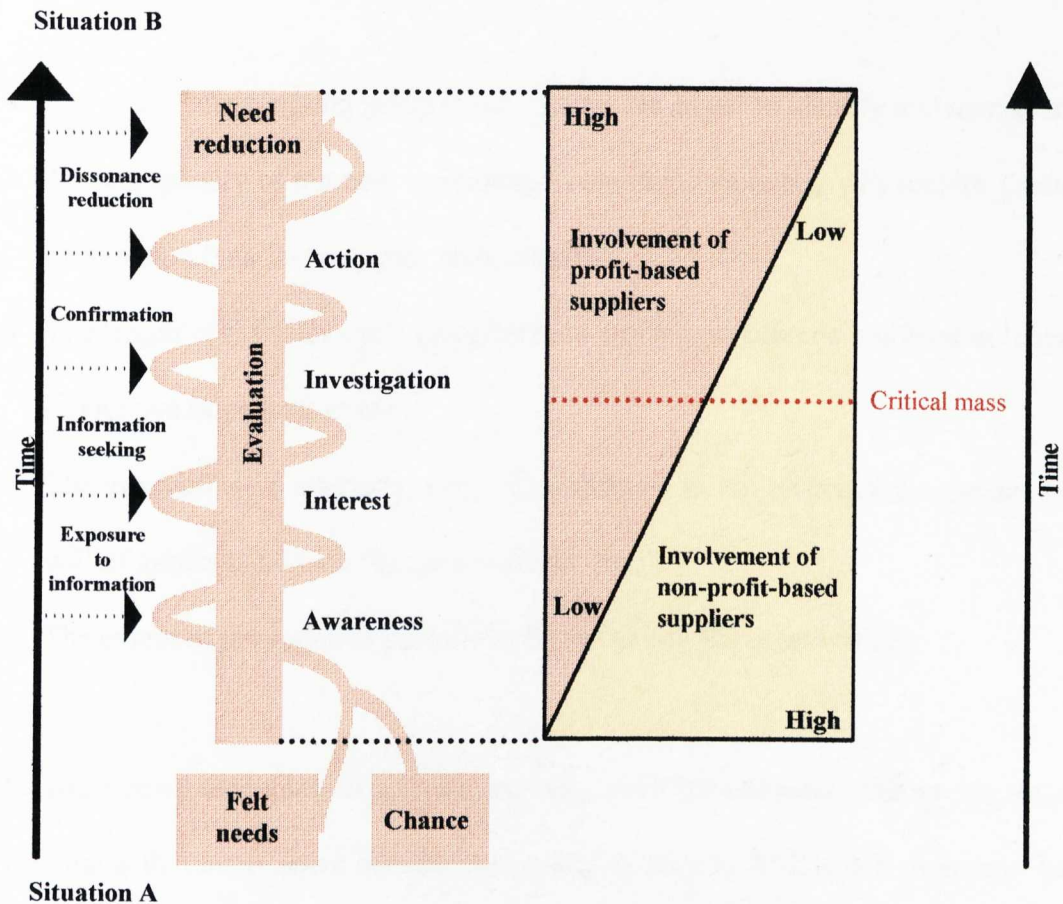


Figure 11-1. Amalgamation of market and adoption models

The critical-mass point can be defined as the point at which the adoption of the technology by a particular group is sufficient to make it viable for suppliers to market to them. The situation is then self-sustainable. Up to the point at which a critical mass of adoption is reached, it must be assumed that the predominant advocates of the new technology to the potential adopters will be non-profit organisations such as government departments and trade associations. Once a critical mass of adoption is reached, the role of such organisations can reduce, as normal market forces come to bear on the adopting group and its suppliers. The point at which a critical mass will be reached will vary according to the proposed technology and the nature of the adopting group. It will be influenced by a number of factors including:-

- The size of the adopting group (small groups are easier to identify and market to)
- The complexity of the new technology (complex technology will require greater initial explanation than less complex technologies)
- The length of the sales cycle (suppliers are unlikely to become involved in lengthy, non-productive sales initiatives)
- The availability of alternate, easier new markets to the technology suppliers (suppliers will of necessity address the easy markets first)
- The extent of intervention performed by the non-profit organisations

So while some technologies and markets may reach critical mass without any intervention, it remains that many more complex technologies such as ASICs will require a 'kick-start' from non-profit making organisations. This need should be considered in the generation of representative models of the adoption process.

11.4 Areas for future study

In the course of this study a number of interesting areas arose which, though not immediately relevant to the subject and scope of this study, raised some interesting questions that might fruitfully be explored in the future. These areas include:-

- A more accurate estimation of the size and nature of the UK SME manufacturing base than is available through government statistics and inference
- A more detailed study of the progression of UK company structure from its traditional form to a more networked structure
- A more detailed study of individual SME companies in S.E.Asia in relation to their perceptions and adoption of microelectronics
- A more detailed study of the success or otherwise of the extensively interventionist industrial policies evident in the Far East.

While not immediately relevant to the adoption of ASICs in the UK, these studies might be key to a better understanding of the general state of the UK manufacturing base, and of the apparent success of the 'Tiger Economies'.

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APPENDICES
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